HUMAX STB

Service Manual

SuperSet

For Model

F1

F1-CI

F1-VA

F1-VACI

HUMAX Super-Set Specification

1 Brief Specifications

Items	Description
Transport Specification	● MPEG-2 transport stream ● DVB compliant SI
Input Frequency	● 950 – 2150MHz
MCPC and SCPC	● Supported
Modulation Type	● QPSK
FEC	● Multi convolution coding supported defined in DVB
PC Card slot	● 2 PCMCIA type-I or II supported common interface in DVB document A017
Smart Card slot	● 2 slot support
LNB Power	● Switchable 13.5 – 18V
0/12V DC output	● Supported, current 100mA
DiSEqC Bus	● DiSEqC 1.0 , 22KHz tone
Video Compression	● MP@ML in MPEG-2
Aspect Ratio	● 4:3 and 16:9 with pan vector
Video Output	● CVBS / RGB
Audio Mode	● Mono ,dual, stereo and joint stereo
Audio Sampling	● 32, 44.1 and 48KHz
Data Service	● Low-speed(RS-232) and high speed
Internal modem slot	● V.32bis,
Flash Memory	● Base 2MB, Extended 1MB
RAM	● Base 2MB
EEPROM	● 128KB / 256KB
On-Screen Display	● 16 colors
Teletext	● Support in DVB ETS300472
Subtitling	● Support in DVB A009
IPPV, EPG	● Supported

2 Electrical Characteristics

2.1 Power Supply

Items	Description
Input Voltage	● 190V – 250V AC
Frequency	● 50Hz
Type	● PWM LINEAR POWER
Power Consumption	● 40W max.
Standby power consumption	● ≤15W
Protection	● Separate internal fuse ● The input shall have lighting protection

2.2 Tuner

Items	Specifications
One Connector	● IEC 169-2, female(F type) ● For signal input from the antenna and LNB
The other connector	● IEC 169-2, female(F type) ● For signal output to an external equipment
Frequency range	● 950 – 2150MHz
No. of inputs	● 1
Signal level	● -25 ~ -65dBm
LNB input	● 75Ω unbalanced nominal impedance ● input return loss >7dB
LNB output	● 75Ω asymmetrical impedance ● output return loss >8dB
LNB power & feed-horn polarization	● Vertical : +13.5V ● Horizontal : +18V ● Voltage tolerance : < ± 0.5V ● Internal DC source resistance < 0.5 ● Current : 400mA max. short circuit protection
LNB Control	● DiSEqC 1.0 ● 22KHz tone ● 0/12V DC output(100mA max. short circuit protection)
Protection	● 4.5KV surge protection, short circuit protection
Bypass(loop-through)	● Power bypass

2.3 RF modulator

Items	Specifications
RF input	● Connector type : IEC 169-2, male ● from terrestrial antenna
RF output	● Connector type : IEC 169-2, female
Impedance	● 50Ω asymmetrical, return loss ≥ 8dB
Bandwidth	● Channel 21-69 for the Demodulator output
TV standard	● PAL-B/G/I
Vision output	● DSB
Audio signal control	● Controllable for volume and mute
Sound output	● 50 μsec pre-emphasis characteristic, digitally processed

3 Channel Processing

This specifications is based on 'Digital broadcasting systems for television, sound and data services; Framing structure, channel coding and modulation for 11/12 GHz satellite services, prETS300 421

3.1 QPSK Demodulation

Item	Description
Modulation	● QPSK
Input symbol rate	● 2 – 31 Mbps

3.2 FEC

Item	Specifications
Inner FEC	● Convolutional code rate 1/2, 2/3, 3/4 5/6, and 7/8 with constraint length ● K = 7
Convolutional deinterleaver	● Convolutional deinterleaving with I = 12
Outer FEC	● Reed Solomon code, RS(204, 188, T=8). ● Quasi error free output is assumed (i.e. BER of about 10^{-11}) in the presence of input error bursts at a BER of 2 x 10^{-4} or better with interleaving depth I=12. In case of worse BER situation, the IRD shall stop the MPEG decoding.
Energy Dispersal Removal	● The polynomial for the Pseudo Random Binary Sequence(PRBS) generator is: $1 + X^{14} + X^{15}$ ● The initialization sequence shall be the 15 bit sequence: "100101010000000"

4 MPEG Decoding

4.1 Demultiplexer

Item	Description
Input transport stream	● MPEG-2 ISO/IEC 13818-1 transport stream specification
Input rate	● 60 Mbit/sec max.
Filter	● One audio PID ● One video PID ● 30 general purpose PIDs
Transport buffer	● A 512-byte buffer for each of the two output elementary streams (audio/video)
Section layer filtering criteria	● Table ID ● Version number ● Section number ● Current/next indicator
Error detection	● CRC32 on all 30 general purpose PIDs
Etc.	● Detects and handles errors, lost packets, and discontinuity ● Spontaneously detects and handles splice points ● Provides PCR recovery ● Provides a high speed output data port for transport packets

4.2 Video Decoding

Items	Description
Profile, Level	● ISO/IEC 13818-2 , MP@ML
Frame rate	● 25 Hz
Aspect ratio	● 4:3, 16:9
Pan vectors	● To allow a 4:3 monitor to give a full-screen display of a 16:9 coded picture

Resolution	● 720 x 576, 25 frame per second
Up conversion to produce a full-screen display	● 544 x 576, 25 frames per second ● 480 x 576, 25 frames per second ● 352 x 576, 25 frames per second, ● 352 x 288, 25 frames per second
OSD	● 16 colors ● Western European character set

4.3 Audio Decoding

Item	Description
MPEG	● MPEG-1 Layer I and Layer II
Mode	● MPEG-1 single channel ● MPEG-1 dual channel ● MPEG-1 joint stereo ● MPEG-1 stereo
Sampling rate	● 32, 44.1, and 48 kHz

5 Mechanical Characteristics

5.1 Front Panel

5.1.1 Key Button

Item	Description
Standby	● Standby/Operation
Channel	● 2 keys for channel up and down

5.1.2 Display

Item	Description
7-segment	● 4-digit ● With decimal dots ● Visible from at least 7 m

5.2 Rear Panel Input, Output

Item	Description
Power code	● Connector type: IEC83, C5 alternative II
Base Band A/V	● Cinch (Video, Audio L+R)
LNB in	● From the LNB ● Connector type: F-type, female
LNB out	● 75Ω asymmetrical impedance ● output return loss >8dB
Terrestrial antenna input	● From terrestrial antenna ● Connector type: IEC 169-2, female
Terrestrial antenna output	● To TV ● Connector type: IEC 169-2, female
SCART	● EN50049 –1

	● TV SCART (RGB, CVBS, Audio L+R output, CVBS, audio L+R input) ● VCR SCART(RGB, CVBS, Audio input, CVBS ,fixed level audio L+R output)
DC12V output	● 0/12V 100mA short circuit protection
Power switch	● power IN/OUT Control
Serial port	● 9-pin D type, 115200bps

5.3 RCU

Item	Description
Operating distance	● 0.2 to 7 m
Angle	● 90° in the horizontal plain, and a vertical offset of ±20°
Keys	● Menu ● Numerical key pad (0 ~ 9) ● TV guide ● 4 cursor control keys (up/down/left/right) ● Select/OK key ● Audio mute key ● Standby key ● TV service ● Subtitle selection ● Audio service ● Audio soundtrack selection ● Exit ● 예비 : 4keys (P+, P-, V+, V-)

6 IRD Interface

6.1 Serial Interface

Item	Description
Electrical interface	● Complying with RS232C specifications
Speed	● 4800,9600,19200(RS232 standards)
More over	● 38400, 57600, 115200 Baud-rate
Flow control	● Hardware flow control by signal DSR and DTR

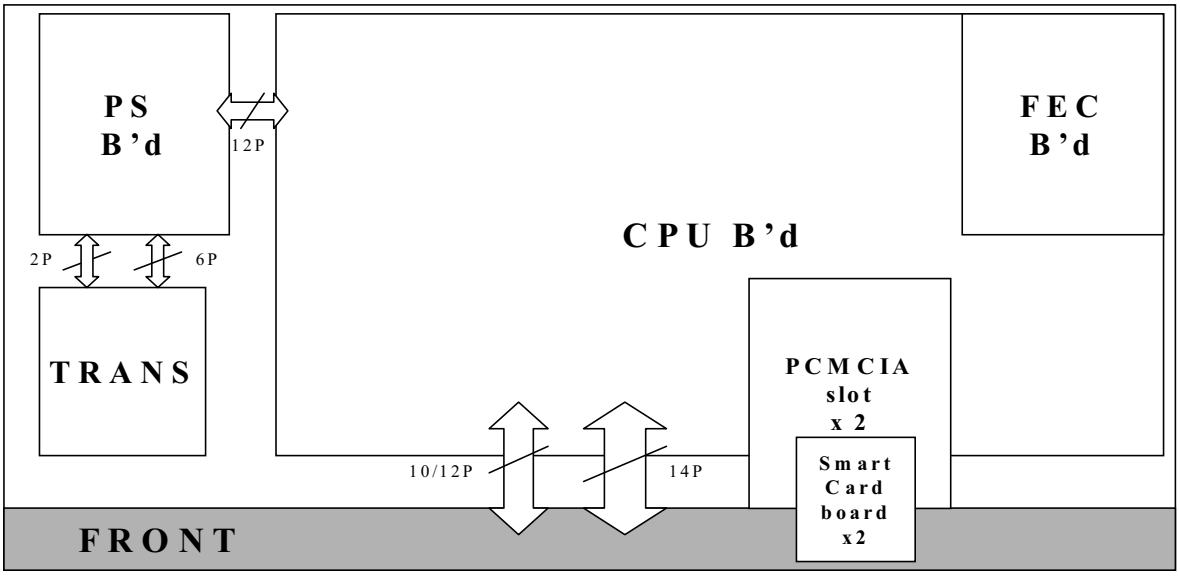
7 Environmental Requirements

Item	Description
Storage	● -10° - +50 °C
Ambient operating temperature range	● 0° - +45 °C
Storage humidity range	● 5 – 95% RH non condensing
Operating humidity range	● 10 – 95% RH non condensing
EMC requirements	● Meet applicable EMC requirements

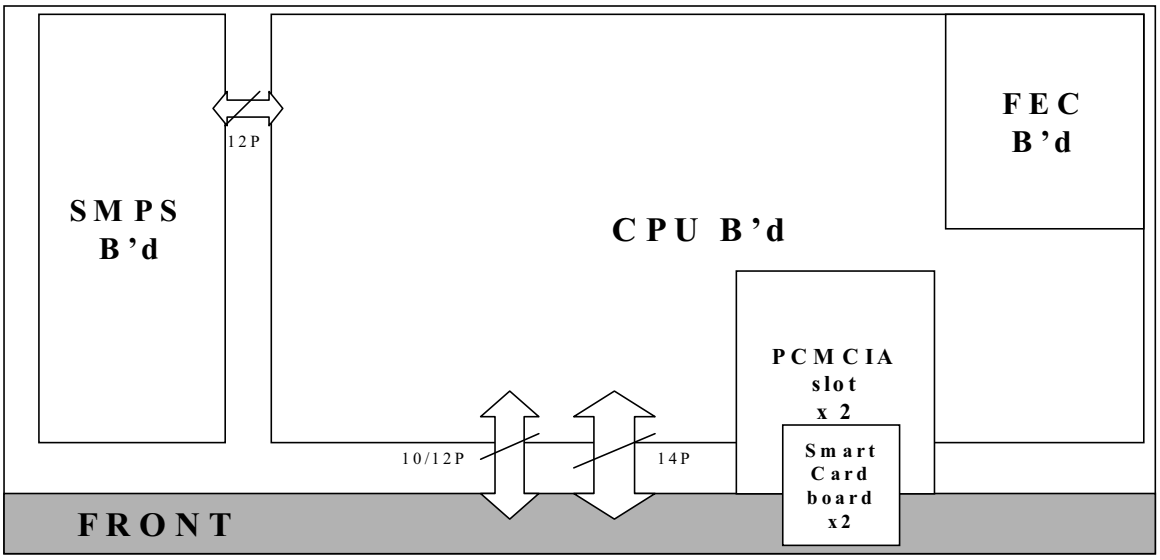
8 Man Machine Interface (MMI)

- Support for MPEG-2/DVB Compliant SI with guidelines on implementation and usage of service information (TM1324 of DVB Doc.)
- Support for Guideline for implementation and use of the common interface for DVB decoder applications
- Support for DVB document A017
- User friendly error messages
- TV, radio modes
- Sub-titling supported
- On-Screen Display for IRD configuration and set-up
- Signal strength and error rate on screen displays
- Context sensitive help messages
- Navigation between channels and programs
- Favorite channel selection
- Parental lock facility by channel and program event
- Support for auto tuning channels
- Support for skipping channels
- Support for different national languages (English, Dutch, German, French, Italian,, Spanish)
- Multiple Network
- Automatic Channel Searching

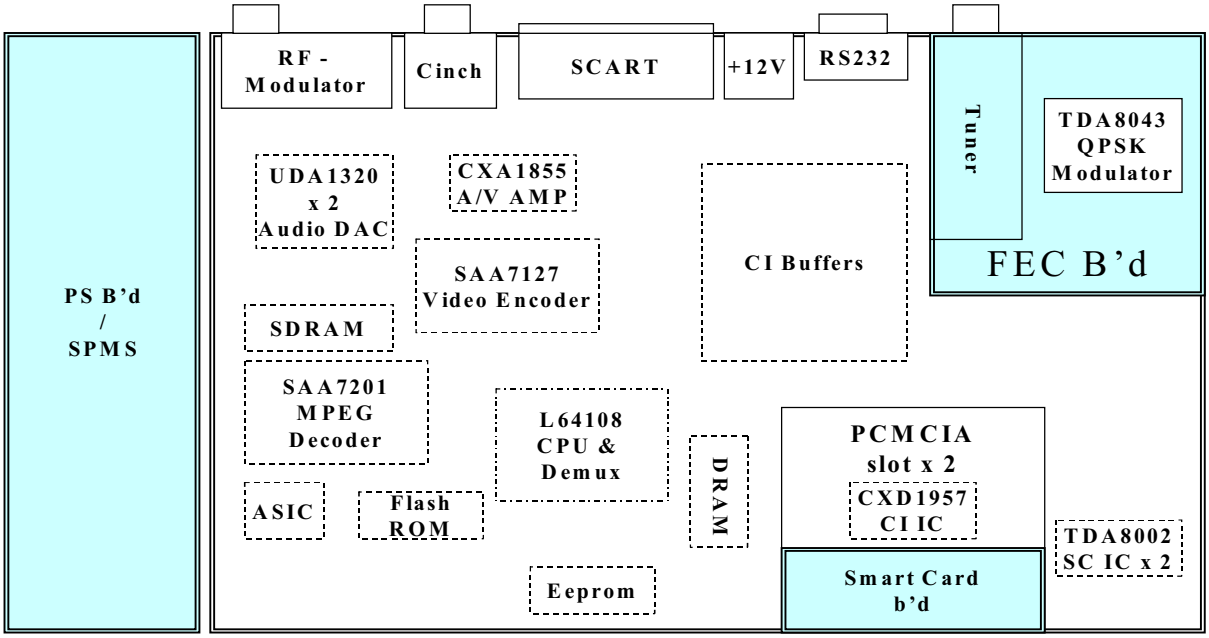
• **Wiring Diagram (with PWM Power)**



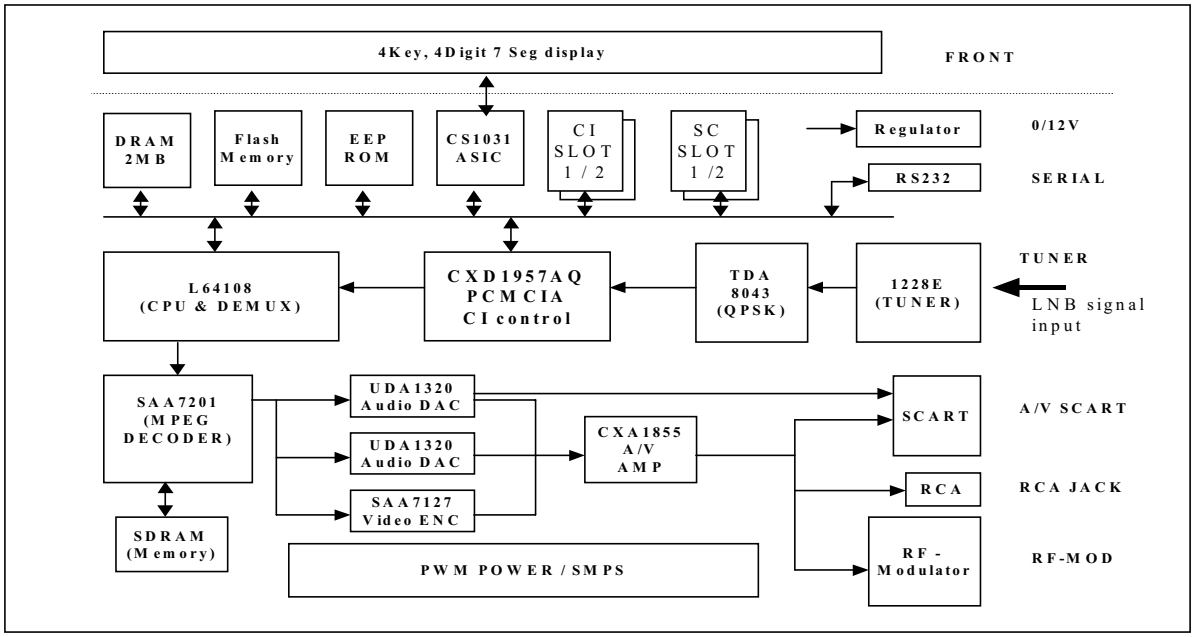
• **Wiring Diagram (with SMPS)**



• Main Board Diagram



• H/W Block Diagram



Parts & Functions (by each schematic diagram page)

Page	Main Parts	Key Functions	Remarks
2	1. Power Regulator - U800, 801, 802, 803, 804, 808	Supplies +3.3V, +5V, +15V, +7.5V, +30V, LNB (Transformer model)	Check that the Transformer model power is defective.
	2. Rectification Diode - D803, 804	Rectifies the transformer input power (Transformer model)	
	3. Other resistance & Tr	Q801 – LNB Power on/off Q800 – 13.5/18V Switching (LNB) (Transformer model)	
6, 7	FET(IRF7303), Tr C108, C125	Supplies CI Power U18 – CI Power Switching C108, 125 – Determines Power Rising Time	Check that the CI initialization fails.
3	1. Tuner and 22K Tone	TN801, Q801, L601, R601 - Receives/Tunes Channel, LNB power supply - Generates 22KHz Tone	Check for the power size and 22K Tone Caution: Stage of generating heat
	2. QPSK Demodulator	U603 – TDA8043, Channel Locking	Be careful in troubleshooting the weak part of the static electricity.
	3. Resistance & Tr	Q604 : Senses LNB Over-load K601 : Connects LNB power	Check that the system operation fails.
	3. Glue Logic Part	U604 : D-FF U606 : NOR Logic	Check CI fails
6, 7	PCMCIA CI CAM	U26 : CI Control IC Various TTL : TS Path U27, U28 : CD and ACK processing parts	Check CI fails
10	1. MPEG TS Demux	U4 : Demux - MPEG TS Signaling	The PLL part is particularly weak in static electricity.
	2. VCXO & Others	U2, 3 : Generates 27MHz system clock	Range of frequency fluctuation by voltage: approx. 100ppm.
11	DRAM - KM416V1204AT-60	System Main Memory	
12, 13	EEPROM (128K	U51 : 128	Loader S/W
14, 15, 16	Flash Memory & Boot ROM Connector	U45 : 2MB, U46 : 1MB Caution: Optional resistance	Main S/W
17	ASIC Reset IC	U10 : CS1031 ASIC (Reset Control, Remocon Input, Front Display, IIC Control, Chip Select) U9 : Reset IC	Related to System Reset
19	MPEG Decoder - U11, SAA7201	Decodes the MPEG Data and then outputs with the digital A/V signal.	Related to System Reset

20	SDRAM - U12	Memory for MPEG Decoder	
21	Video Encoder - U21, SAA7127B	- Outputs after converting Digital Video Data to Analog Video Data. - Tele-Text Data Processing	Related to Video Output
	EMI Filter	- F2~5 : 27M filter for EMI	
22	Audio DAC - U16, U17 : UDA1320	- Outputs after converting PCM Audio Data to Analog Audio U16 = TV SCART, RF, CINCH U17= VCR SCART	Related to Audio Output
	OP-AMP Stage - U40, 41 : TL072	- Inverted amplification of DAC audio signal	
23, 24	U49, U50 - IC Card Interface	- Smart Card Interface - Embedded CI	VA De-scramble
27	Video Filter	- Connects and filters the video signal	Related to Video Output
28	5V(A) Generator - U406	SCART & RF Supply	
29	A/V AMP & Mux - U400(CXA1855) Buffer - Q400~405	- Gain: 6dB (Video), 0dB(Audio) - Buffer: Increase in output	Related to A/V Output
30	SCART Function - U401 - Various Signal Tr : Function of Pin 8, 16	Control Signal definition - SCTFO : On as VCR by-pass - WIDE : On as wide mode selection - BLANK : On (RGB), Off (CVBS) - SEL : Status out of VCR by-pass - VCR : On as VCR by-pass Off	Pin 8 (SWITCH) 9.5~12V=4:3 mode 5 ~ 8V =16:9 mode 0 ~ 2V = By-pass Pin 16(BLANK) 1 ~ 3V = RGB 0 ~0.4V=CVBS
31	RF-Modulator - U402	U401 – Transmits to TV after converting A/V signal to UHF vs. signal. Q414, 415, 416 – Converts to mono signal after mixing Audio L/R signals	Noise occurs in the upper channel (because of a defective modulator)
32	Phone Jack – JP401 Buffer – Q413	Outputs CVBS and Audio L/R R458, 459, 460: Adjustment of impedance	Related to CINCH Output
33	12V Generator – U404 DC Jack – JP402	Generates LNB Switching voltage (0/12V)	
34	232 Interface - U405 232 Port – JP403	I/P chip and connector (for UART communication)	Serial Communication Port

Classification	Guide for Troubleshooting	Section	All model with Super Set

- The following work flow is recommended when troubleshooting.

1. Appearance Check
   - Check for the state of set assembly, connection of connectors, curved or broken PCB, soldered/shorted parts, and other noticeable defective parts.

2. Power Supply Stage Check
   - After applying power to the set, check for the circuits from the primary AC input of transformer through the output power supply (including +3.3V DC). The output power supply of Super Set model is as follows
     : Digital Power Supply (+3.3V, +5V)
     : Analog Power Supply (+7.5V, 15V)
     : LNB Power Supply (+13.5V/+18V), VT(+30V)

3. System Check
   - Check L64108(CPU) works normally; i.e., check for the items such as System Reset, System Clock, Memory , and other various Parallel Device Access that are essential when the set operates. First of all, the operating power supply from each functional device must be checked.

4. Channel Check
   - Check for the part which receives, tunes, and locks the RF frequency output from LNB(antenna) and then outputs the DC power supply of driving LNB and 22KHz Tone signal. Check also the TS(Transport Stream) signal output from QPSK Modulator(TDA8043) operates.

5. PCMCIA Common Interface Check
   - The CAM card must be inserted when decoding the channel scrambled under CI Format. When inserting, proceed in the following sequence: Card Detect, CAM Power On, CAM Initial. By this proceeding, TS Stream Input Buffer, CAM Output Stream and TDA8043 Output Stream are switched and then input to L64108(Demux). So check for the part relating to the stream of TS signal.

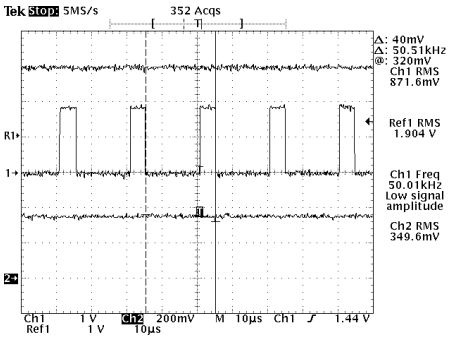
6. MPEG & AV Check
   - Check form MPEG Decoding through A/V output. And then check for the functions of the output terminals of Back Panel (SCART, RF-Modulator, Phone Jack).

- The figures shown in the guide depend on the status of system, received signal, or etc.

- When a problem happens, the point is to find where it takes place by tracking the stream of the signal related. Therefore, the waveforms shown herein are recommended only as a pattern of the signals related.

Classification	Basic Check Item – Power Supply	Section	PWM Power (PS) B'd
Item: Digital power supply +3.3V			
Symptom: System Doesn't Operate			

- Measurement: The input/output voltage waveform of System Main Digital Power Supply (+3.3V) is as shown the figure below.



☐ Waveform Description
1) U803(LM2576) Input : +20V
2) U803 Output (Switching)
3) +3.3V output

☐ Location of Measurement: See Schematic Diagram page 2/36
1) D804 (+) pin
2) D806 Anode
3) C812 (+) pin or R820

☐ Outline: Description of each measurement is as follows.

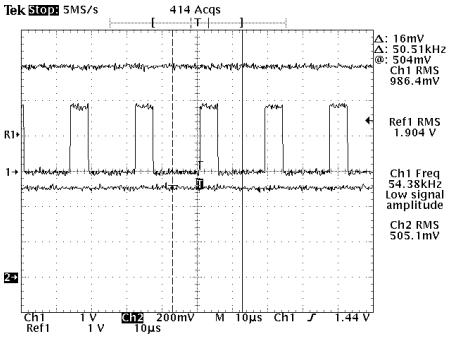
✓ U803 Input: The secondary voltage of Transformer is rectified and then output via D804 (+) pin. At this time the voltage is about 20V. If this voltage is not measured, check both D804 and Transformer outputs.
✓ U803 Output: The U803 output becomes Switching Waveform with a fixed duty. If this waveform is not output, check for the solder of the circuits associated to LM2576.
✓ +3.3V Output: The voltage must be more than 3.4V so that the system can operate securely. If the voltage is less than 3.4V or any abnormal voltage is generated, check for the solder of R820.

- General causes of failure
  - PCB Pattern Short
  - Component Soldering Short
  - Defective Parts

- Countermeasures: Parts Replacement / Re-Soldering / Application of ECO

Classification	Basic Check Item – Power Supply	Section	PWM Power (PS) B'd
Item: Digital Power Supply (+5V)			
Symptom: System Doesn't Operate			

- Measurement: The input/output voltage waveform of System Main Digital Power (+5V) is as shown the figure below.



☐ Waveform Description
1) U804(LM2575) Input: +20V
2) U804 Output (Switching)
3) +5V output

☐ Location of Measurement: See Schematic Diagram page 2/36
1) D804 (+) pin
2) D807 Anode
3) C815 (+) pin or R818

☐ Outline: Description of each measurement is as follows.

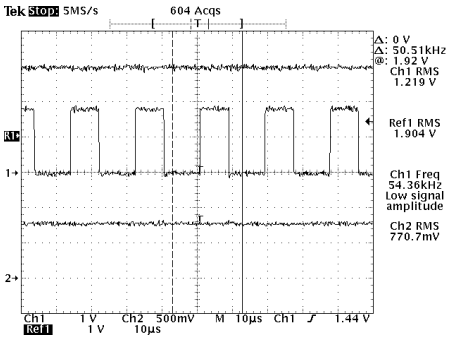
✓ U804 Input: The secondary voltage of Transformer is rectified and then output via D804 (+) pin. At this time the voltage is about 20V. If this voltage is not measured, check both D804 and Transformer outputs.
✓ U804 Output: The U804 output becomes Switching Waveform with a fixed duty. If this waveform is not output, check for the solder of the circuits associated to LM2575.
✓ +5V Output: The voltage must be more than 4.5~5.5V so that the system can operate securely. If any abnormal voltage is generated, check for the solder of the feedback resistor R818, R819.

- General causes of failure
  - PCB Pattern Short
  - Component Soldering Short
  - Defective Parts

- Countermeasures: Parts Replacement / Re-Soldering / Application of ECO

Classification	Basic Check Item – Power Supply	Section	PWM Power (PS) B'd
Item : Digital Power Supply (+7.5V)			
Symptom: System Doesn't Operate			

- Measurement: The input/output voltage waveform of System Main Digital Power Supply (+7.5V) is as shown the figure below.



□ Waveform Description
1) U802(LM2575) Input: +20V
2) U802 output (Switching)
3) +7.5V output

□ Location of Measurement: See Schematic Diagram page 2/36
1) D804 (+) pin
2) D805 Anode
3) C810 (+) pin or R809

□ Outline: Description of each measurement is as follows.

✓ U802 Input: The secondary voltage of Transformer is rectified and then output via D804 (+) pin. At this time the voltage is about 20V. If this voltage is not measured, check both D804 and Transformer outputs.

✓ U802 Output: The U802 output becomes Switching Waveform with a fixed duty. If this waveform is not output, check for the solder of the circuits associated to LM2575.

✓ +7.5V Output: This voltage must be more than 7.5V so that system can operate stably, peculiarly for the prevention of error at the A/V part. If any abnormal voltage is generated, check for the solder of feedback resistor R815, R816.

- General causes of failure
  - PCB Pattern Short
  - Component Soldering Short
  - Defective Parts

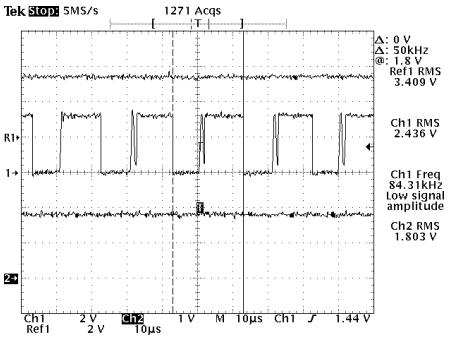
Countermeasures: Parts Replacement / Re-Soldering / Application of ECO

Classification	Basic Check Item – Power Supply	Section	PWM Power (PS) B'd

Item: LNB Power Supply (13.5V/18V)

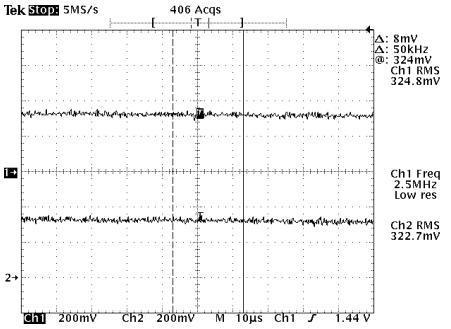
Symptom: TS Locking Doesn't Work (No or Bad Signal is OSD displayed)

- Measurement: Two types of LNB voltages are generated according to Antenna Setting Mode
  - Horizontal type = 18V, Vertical type = 13.5V



- ☐ Waveform Description
  1) U801(LM2574) Input: +35V
  2) U802 Output (Switching)
  3) LNB Voltage Output(13.5/18V)

- ☐ Location of Measurement: See Schematic Diagram page 2/36
  1) D803 (+) pin, Pin1
  2) D802 Anode
  3) C804: (+) pin or C805



- ☐ Waveform Description
  1) LNB_HOR: Horizontal Antenna Select
  2) LNB_ON: LNB Power Supply Enable

- ☐ Location of Measurement: See Schematic Diagram page 2/36
  1) Contact of R811 & R812 (+3.3V)
  2) Contact of R813 & R814 (+3.3V)

☐ Outline: Description of each measurement is as follows.

✓ U801 Input: The secondary voltage of Transformer is rectified and then output via D803 (+) pin.
✓ U801 Output: Switching waveform with a fixed duty which is proportional to voltage size
✓ LNB Voltage: Check LNB operating power supply meets ± 0.5V.

- General causes of failure
  - PCB Pattern Short
  - Component Soldering Short
  - Defective parts

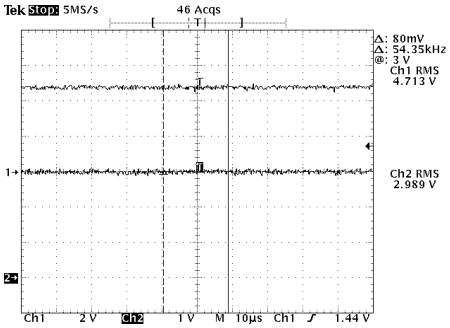
- Countermeasures: Parts Replacement / Re-Soldering / Application of ECO

Classification	Basic Check Item – Power Supply	Section	PWM Power B'd

Item: Power Supply VT (+30V) / +15V

Symptom: No Tuner Locking or Picture Broken after Locking
Error happens in SCART output, CI initialization, or DC 0/12V conversion

- Measurement: More careful check is required when any problem happens because a tuner responses sensitively according to ripple, range of voltage. The schematic measurement waveform relating to VT is as shown in the figure below.

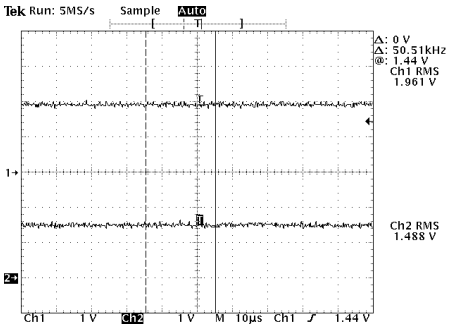


- ☐ Waveform Description
  1) U800(LM317) Input: +48V
  2) U800 Output (VT voltage): +30V

- ☐ Location of Measurement: See Schematic Diagram page 2/36
  1) D800 Anode
  2) R804

- ☐ Outline: Range of VT is approximately 28 ~ 31V DC. If the measurement value is out of this range, check R802, R803, and U800 are correctly inserted/soldered.

- Measurement: +15V is an operating power of SCART, CI FET Gate, DC 0/12V. The measurement waveform of associated circuit is as shown in the figure below.



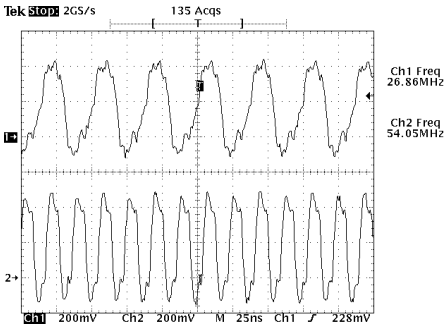
- ☐ Waveform Description
  1) U808(LM7815) Input: +20V
  2) U808 Output : +15V

- ☐ Location of Measurement: See Schematic Diagram page 2/36
  1) D804 (+) pin
  2) C817

- ☐ Outline: If the measurement value is out of this range, check the device is correctly inserted/soldered.

Classification	System Check Item	Section	CPU B'd
Item: System Clock (27MHz) and L64108 Internal Clock(54MHz)			
Symptom: System Doesn't Operate Or operates intermittently			

- The system clock mainly depends on the security of VCXO. It will be further described in the item L64108 Reset .
- L64108 internal clock is twice 27MHz System Clock (54MHz). It is generated by PLL inside 108 and used to operate L64108.
- This is peculiarly sensitive to static electricity. So this might become a cause of easily producing failure.
- The waveforms of two clocks are as shown the figure below.



□ Waveform Description
1) System Clock (27MHz)
2) Internal Clock (54Mhz)

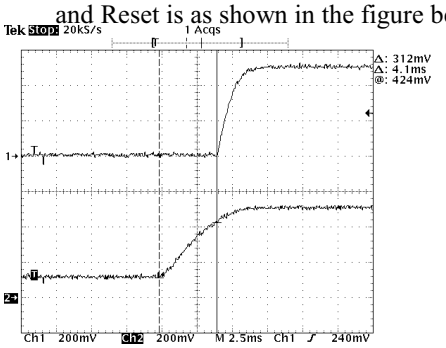
□ Location of Measurement: See Schematic Diagram page 10/36
1) U4(L64108) Pin 7
2) U4(L64108) Pin 20

- Causes of Failure & Countermeasures

- The 24MHz clock is a basic system clock. If it is not secure, check for the insertion of circuits associated to VCXO. Especially, the presence of an optional resistor (R24) according to the type of VCXO must be checked.
- If the 54MHz clock operates insecurely, parts replacement is recommended (because instability happens mostly when PLL of L64108 is damaged by static electricity and others).
- When replacing parts, be careful not to be injured by static electricity coming from a soldering iron.
- Check for the status of assembly/solder and wrong or inverse parts insertion

Classification	System Check Item	Section	CPU B'd
Item: Main Reset & System Reset			
Symptom: Power On Reset Doesn't Work System Malfunction Happens.			

- Measurement: Timing between operating voltage and reset needs to be checked because it may affect the operability of device. The measurement waveform between L64108 power supply and Reset is as shown in the figure below.



- ☐ Waveform Description
  1) Reset Signal
  2) +5V Power Supply

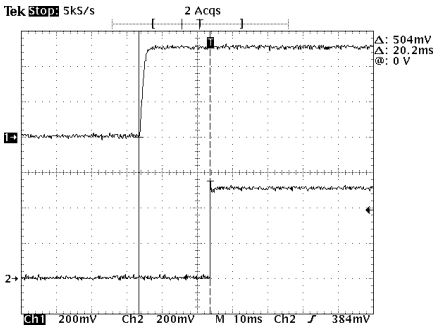
- ☐ Location of Measurement: See Schematic Diagram page 17/36
  1) U19(KIA7042P ; Reset IC) Pin3
  2) U10(CS1031 ; ASIC) Pin6

☐ Outline: SuperSet Reset occurs due to +5V. Reset happens when U19 input threshold voltage exceeds the fixed voltage (4.2V). Time Delay is a process for applying Reset after the operating power supply is stabilized. If the reset signal is not generated, check for time delay.

- Reset Procedures
  1) First, the primary delay happens due to +3.3V/+5V Timing. And then the secondary delay takes place because of the threshold voltage of Reset IC and the delay inside ASIC.
  2) SAA7201(MPEG Decoder) is completed by Main Reset. About 20msl later, L64108 is reset by System Reset (ASIC pin 6 (RESET)).
  3) Reset must be released after the operating power supplies (+3.3V & +5V) are stabilized.
  4) Because the clock of each device needs some time to be stabilized.

- Causes of Failure & Countermeasures
  1) For Main Reset, timing can be distorted by defective U9. And also any malfunction can happen because the contact of TACT SW, S1 fails.
  2) Check for the output from FET (see Schematic Diagram page 5/36) connecting the power supply of CPU B'd . And also check for the insertion of related devices.

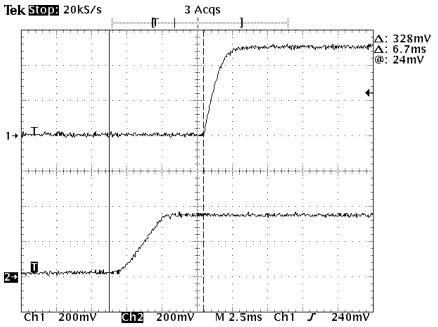
Classification	System Check Item	Section	CPU B'd
Item: Main Reset & System Reset			
Symptom: Power On Reset Doesn't Work System Malfunction Happens			

- Measurement:. Timing between operating voltage and reset needs to be checked because it may affect the operability of device. The measurement waveform between Main Reset and System Reset is as shown in the figure below.
- 

  - Waveform Description
    1) Main Reset Signal
    2) System Reset Signal
  - Location of Measurement: See Schematic Diagram page 17/36
    1) U19(KIA7042P ; Reset IC) Pin3
    2) U10(CS1031 ; ASIC) Pin6

- Outline: SuperSet Reset timing happens due to the delay inside +5V threshold and ASIC
  After the operating power supplies (3.3V, +5V) are stabilized. The above figure shows the waveform of checking the delay inside ASIC (20mS).

- Measurement: The following figure shows the waveform of measuring the delay in rising time of +5V and +3.3V.



  - Waveform Description
    1) Main Reset Signal
    2) +3.3V Power Supply
  - Location of Measurement: See Schematic Diagram pages 5/36, 17/36
    1) U19(KIA7042P ; Reset IC) Pin3
    2) U53(IRF7303 ; FET) Pin1

- Outline: The SuperSet reset timing is completed by +5V, +3.3V rising time. The +5V rising time is delayed by RC time constant (R231 & C201) at FET Gate Stage.

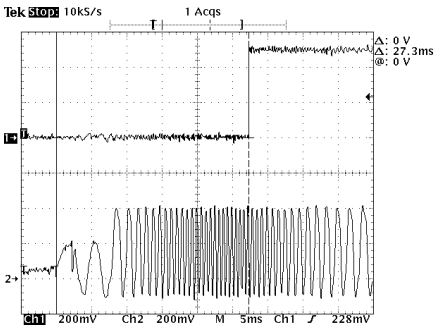
- Causes of failure & Countermeasures

1) For Main Reset, timing can be distorted because of defective U9 . And also any malfunction can happen because the contact of TACT SW, S1 fails.
2) For System Reset, check for the power supply of ASIC(U10) and the status of pin soldered.
3) If the delay of +5V, +3.3V rising time happens, check for the status of RC time constant (R231, C201).

Classification	System Check Item	Section	CPU B'd
Item: System Reset & System Clock			
Symptom: Power On Reset Doesn't Work System Malfunction Happens.			

- System Clock 27MHz must be stable in System Reset or Power On Reset. There are cases where the clock is unstable until System Reset is released in Power On Reset because of a defective VCXO or others.

- Make sure that the waveform as shown in the figure below is provided in Main Power On .



- ☐ Waveform Description
  1) System Reset Signal
  2) 27MHz Clock

- ☐ Location of Measurement: See Schematic Diagram pages 10/36, 17/36
  1) U10(CS1031 ; ASIC) Pin6
  2) F1(FILTER) Pin1

- Causes of Failure & Countermeasures
  - ✓ One of principle causes is a defective VCXO. Replace the part in this case.
  - ✓ In cases other than this, check for the status of assembly, soldering, etc.

Classification	System Check Item	Section	CPU B'd
Item: SAA7201 Operation			
Symptom: MPEG Play Doesn't Work Failed when performing a test on 7201 memory			

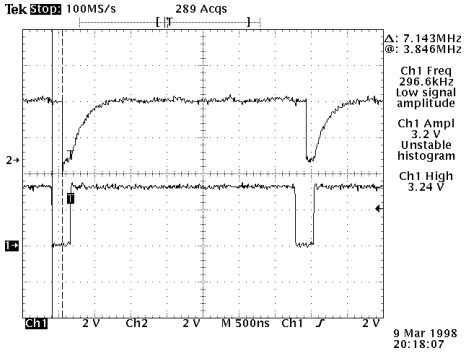
* SAA7201 needs a process of setting the initial reset timing because of Chip Bug (and which is applied to the present circuit). But if 7201 still doesn't operate, check at least the following items to make sure that 7201 itself operates.

Location of Measurement:
See Schematic Diagram page 19/36
Pin 84 of U11

81MHz
Clock

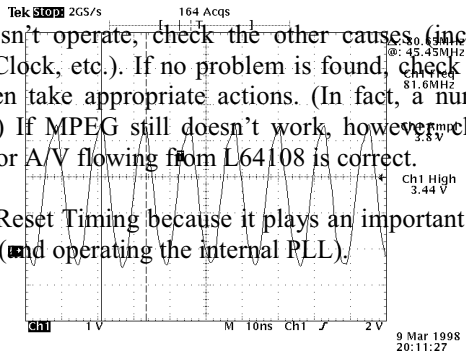
Location of Measurement:
See Schematic Diagram page 8/36
Pin8 of U27

DSACK1



Location of Measurement:
See Schematic Diagram page 5/3
Pin9 of U36

7201CS

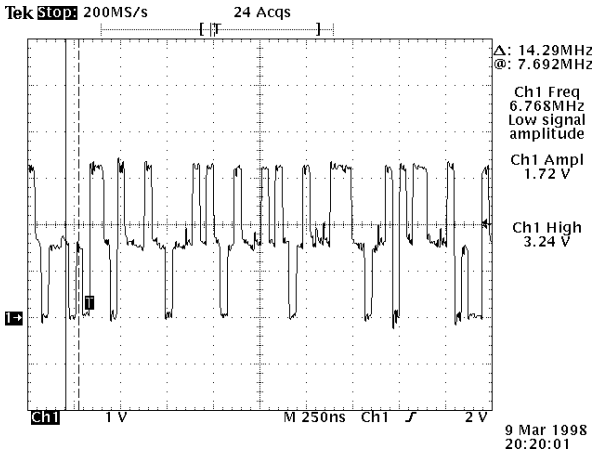


If SAA7201 doesn't operate, check the other causes (including Power Supply (+3.3V), Reset Timing, System Clock, etc.). If no problem is found, check short, cold solder caused by failure in soldering and then take appropriate actions. (In fact, a number of failures happened because of wrong soldering.) If MPEG still doesn't work, however, check all 8 bit lines to make sure that MPEG TS Data for A/V flowing from L64108 is correct.

- Check also Reset Timing because it plays an important role when initializing MPEG Decoder (SAA7201) (and operating the internal PLL).

Classification	System Check Item	Section	CPU B'd
Item: MPEG Video Data Output			
Symptom: Screen color severely blurs or screen is distorted			

- When the system works normally, but the output screen color blurs or screen is distorted, it is mostly because the A/V Data flowing from SAA7201to SAA7127is cut or shorted.
- In this case, check A/V Data Line to find the defective part and then take appropriate actions.. The waveform that is output when shorting between pins is as shown in the figure below.

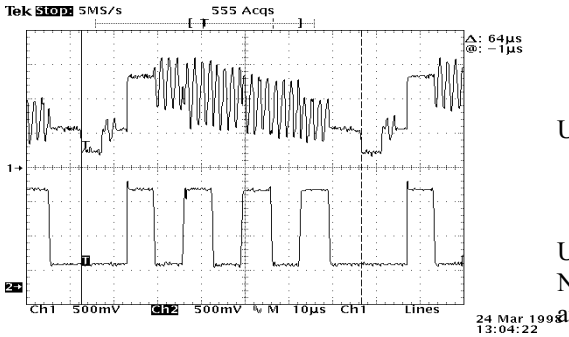


Location of Measurement: Waveform when shorting U11(SAA7201) Pins 109,110

- Video Encoder controls the operation of device via I2C communication. At this time, if I2C Line has any problem, the Video Encoder doesn't operate. Therefore, check that communication is properly made.
- When any system problem happens, the point is to find where it takes place by tracking the stream of the signals related. Therefore, the waveform shown in the figure above should be recommended only as a pattern of the signals related (and check according to the stream of signal).

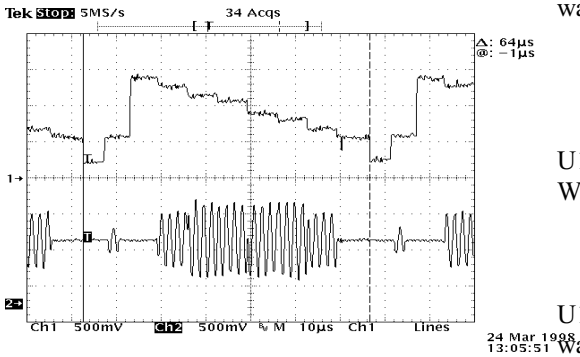
Classification	A/V Check Item	Section	CPU B'd
Item: Video Output			
Symptom: No Video Signal Output			

- When the system works normally, but no video is output through SCART, Phone Jack, RF-Modulator, check first Analog Video is output from U14 (SAA7127) Video Encoder.
- Output from U14: CVBS, SVHS, R, G, B (see the schematic diagram page 21/36). The waveforms as shown in the figure below are output when using an 100% color bar signal pattern.



U14, Pin30 CVBS Output Waveform

U14, Pin29 Blue Output Waveform
Note: The Green/Red output waveforms are different from the Blue output waveform, but they keep this type of waveform.



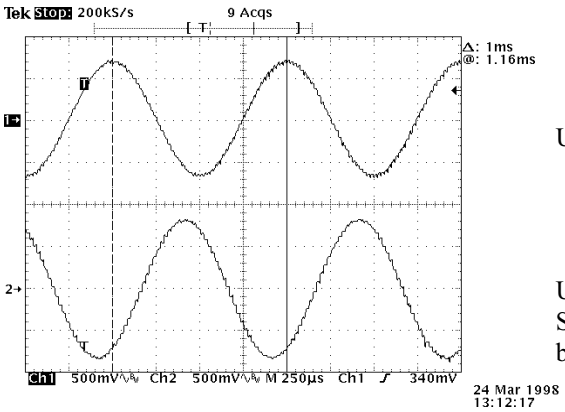
U14, Pin30 SVHS Luma Output Waveform

U14, Pin23 SVHS Chroma Output Waveform

- If outputs from U14 are normally provided, the cause of any problem is mostly the circuits related. Therefore, find the problem by measuring the waveform of each part according to the circuits related to the output stage (such as SCART, Phone Jack,…) where the problem takes place and then take appropriate actions.
- The level of output signal varies according to its location on the circuit. To check the levels of general cases, see the Video Encoder Performance Measurement Table.
- In general cases, it is important to check the input/output signals of Video Encoder (because the principle cause of the failure in the development process was the cold-soldered device).

Classification	A/V Check Item	Section	CPU B'd
Item: Audio Output			
Symptom: No Audio Signal Output			

- If no audio signal is output to SCART, Phone Jack, RF-Modulator, check first two Audio DACs. U16(UDA1320) outputs Audio to TV-SCART, Phone Jack, RF-Modulator and U17(UDA1320) outputs Audio to VCR-SCART.
- Because the output level and characteristic of Audio are sensitive to the values of R, C composing the circuit of U40, 41 (TL072 OP-AMP) stage, it is required to mainly check U40, 41 when the characteristic of a certain part fails.
- The waveforms output from U24, 30 when using an 1KHz Tone signal are as shown in the figure below.



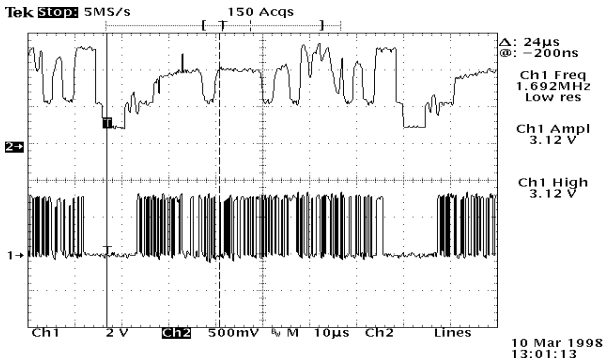
U40, Pin1 Output Waveform

U41, Pin1 Output Waveform
Steps are shown on the waveform because of the characteristic of part

- If audio is normally output from Audio DAC, then check each circuit to find where the problem happens.
- Because No Audio Output relates to the analog audio, it is assumed that most of failures are caused by wrong soldering and parts (Same as video).

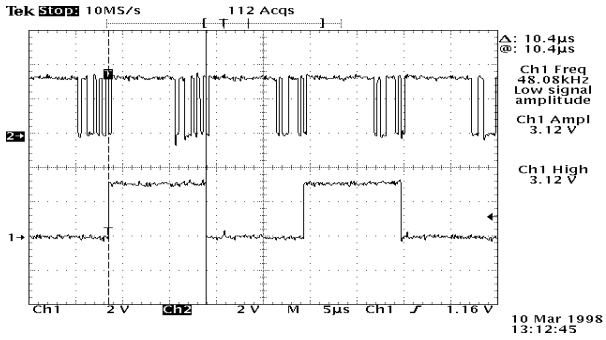
Classification	A/V Check Item	Section	CPU B'd
Item: No A/V Output			
Symptom: System is OK, but No A/V Output			

- If A/V is not output, check first the digital signal input to Video Encoder and Audio DAC is normal. The measurement waveforms of Video Encoder and Audio DAC are as shown in the figure below.
- If the required input waveforms are normal, proceed with the sequence of checking Analog Output.



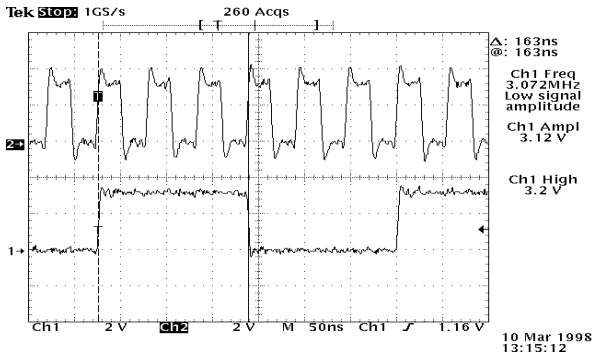
Analog Video Output

Video Data Input (VPD0)
Note the area which is synchronized With video output.



Audio Data Input

LRCLK Input
The LSB Data of Audio Left/Right starts at the rising/falling edge.



ACLK

BCLK

Classification	A/V Check Item	Section	CPU B'd
Item: Function of A/V Amp			
Symptom: System is OK, but No A/V Output			

- The output from Video Encoder is input to U400(CXA1855Q) A/V Amp and then the signal set according to mode is output to SCART, RF Modulator, CINCH. If the output from Video Encoder is OK, check A/V Amp in the following sequence.
  1) Check U400 Power Supply (+7V).
  2) Check for the short or solder between pins..
  3) Check the final input/output is performed via Tr Buffer.
  4) I2C Line Check: Check both CLK and Data operate correctly.

- The output from Audio DAC is split into a level fixed signal and a level controllable signal, and then it is input to A/V Amp. The level fixed signal is output to VCR SCART and the level controllable signal is output to TV SCART and RF, CINCH jack. If Audio DAC Output is okay, check the A/V Amp stage in the same sequence as the video signal follows.

- Audio Mute Function Not Available: It is assumed that Audio Mute doesn't operate because of the following two reasons:
  1) If the operating power supply (+7V) of U400 is less than +7.5V, check the level of power supply because the switching inside CXA1855Q can be affected by mutual interference
  2) I2C Line Check: Check both CLK and Data operate correctly.

- If any noise happens in the video signal, check the filter of the signal which is transmitted to A/V Amp is properly inserted and soldered. (see Schematic Diagram page 27/36).

Classification	A/V Check Item	Section	CPU B'd
Item: Function of SCART			
Symptom: - RGB/CVBS Mode Switching Doesn't Work - 16:9/4:3 Mode Switching Doesn't Work - Bypass Signal Isn't Output			

- If CVBS/RGB Video signal is output, but TV mode switching doesn't work, check TV SCART pin16. The range of operation is provided as follows.
  1. RGB Mode : +1V ~ +3V
  2. CVBS Mode : 0 ~ +0.7V

□ Related parts are as follows.
  R45, Q410, D419 – Switches ON/OFF +5V(A) after receiving Blank Control Signal from U4.
  R448, Q411 – Forces Q410 to be turned OFF when an external bypass signal exists.

- 16:9/4:3 mode switching is done through TV SCART pin8.
  The operating voltage is provided as follows.
  1. TV OFF – 0V : TV is turned OFF when the operating voltage is 0V.
  2. Wide (16:9) : +6V
  3. Narrow(4:3) : +10V ~ +12V

□ Related parts are as follows.
  Q406, Q407,R214 –When SCTFO is '1,' Q406 is turned ON. But Q407 is turned OFF, and so voltage is not output.
  Q408, D421, R444 – When SCTFO is '0' and the wide signal of Q408 is '1,' Q408 and D421 Are turned on. And then D421 zener voltage (7.5V) is output. This is referred as Wide Mode.

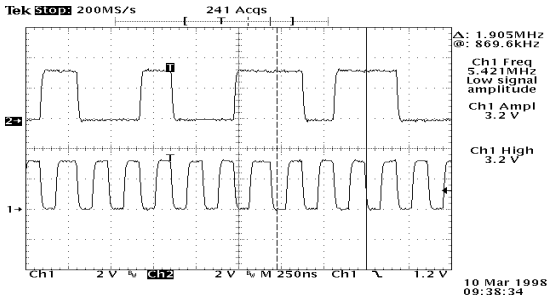
- Bypass Mode: If a certain voltage is input to VCR SCART Pin 8, it is output to TV SCART Pin8 via D417. And then Q409 is turned on via D418. At this time, the voltage output to the emitter of Q409 turns on Q411 and it is sensed at the input port of U4 after passing the 'SEL' signal line via R449 (D422 is a zener diode for preventing overvoltage).

- Q412 is used when turning off Q409 so that Q409 is not affected by the voltage input to VCR SCART pin 8 in Normal Mode.

- In the structure of SuperSet SCART, a matter that requires attention is that the internal function voltage and the bypass voltage are not switched but combined with Diode. 16:9/4:3 voltage is combined with D418, 416 and Blank voltage is combined with D419, 420. This means that the function voltage of TV SCART is affected by the state of VCR operation when VCR is connected to VCR SCART. Therefore, when performing a test on the function voltage, be sure to do only when VCR is not connected to VCR SCART.

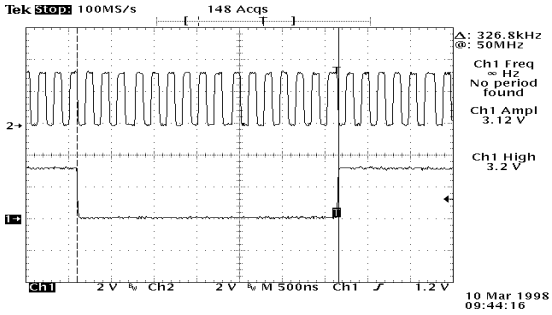
Classification	System Check Item	Section	FEC B'd
Item: TDA8043 Data & Clock			
Symptom: Locking Doesn't Work MPEG Play Doesn't Work			

- Check the following items to see if TDA8043 operates normally against the above two symptoms. Proceed on the assumption that both tuner and L64108 operate normally.



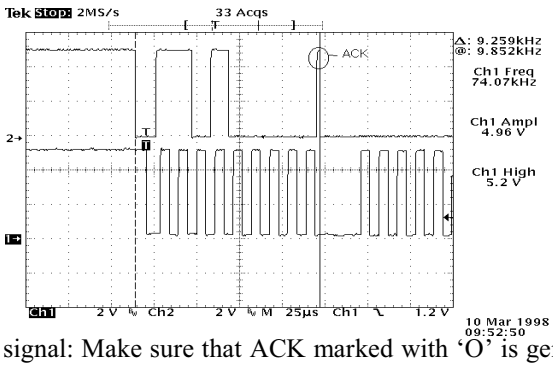
U603, 8043D0

U603, 8043 CLK



U603, 8043CLK

U603, 8043VLD



U603, 8043SDA

U603, 8043SCL

- I2C signal: Make sure that ACK marked with 'O' is generated at the 9th Clock of 8043SCL as shown in Figure 3.

- The other items related to TDA8043 will be further described in the check items related to channel.

Classification	Channel Check Item	Section	FEC B'd
Item: Channel Part Troubleshooting Flow			
Symptom: Items to be checked when troubleshooting Channel Part			

Channel Part Troubleshooting: Tuner and TDA8043 are connected when locking.
So each part to be controlled is described as follows.

1. Tuner (SD1228/LA MK2) Check
   1) Check C607 to make sure the internal operating power is +5V.
      (+4.75 ~ +5.25V)
   2) Check C604 to make sure of Tuner Tuning Voltage (30V) and Ripple.
      (+28.5 ~ 31V / MAX 50mV)
   3) Check LNB Power is turned On and LNB Power is output
      (LNB Power On : +3.3V (HIGH) at R629)
      (Check the voltage of C601 (+) pin is 17 ~ 19V (HOR) , 13 ~ 14V (VER))
   4) Check CC601 (+) pin to make sure 22 ㎑ Tone waveform is generated
      (Signal Type = AC).
      (Amplitude 400~800mV, Duty 45~55%)
   5) Check R609(Tuner Pin 5) to make sure Tuner 479.5 ㎒ Carrier VCO Input voltage is Within 2.4 ~ 2.6V
      Check C609, C610 to make sure Tuner Output I/Q voltage is within 1.9 ~2.0V and its waveform is about 600mVpp

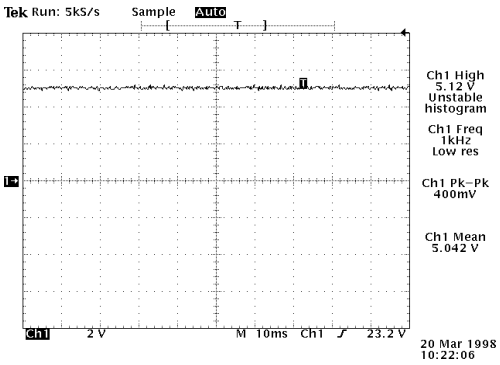
2. QPSK Demodulator (TDA8043) Check
   6) Check C633,C635,C638 to make sure TDA 8043 Power Supply Line is 3.3V (3.2 ~ 3.4V).
   7) Check R616 to make sure TDA 8043 Clock (65 ㎒) oscillate.
      (65,001,900 ~ 64,998,100 ㎐ 30ppm)
   8) Check TDA8043 when turning on I2C Bus Line which is generated when initializing both TUNER and TDA8043. (Pin 53 = Data , Pin 52 = Clock)
   9) Check TDA 8043 Pins 29, 49 to make sure of both BCLK and VLD signals.
      (BCLK is about 5.4 ㎒ and VLD is about 26 ㎑. They can vary according to Symbol Rate)
   10) Check TDA8043 Pin 48 to make sure the PBAD signal is 3.3V(High).
      (The PBAD signal must be HIGH while 8Bit Data is being output.)
      (Locking doesn't work when the PBAD signal is Low or in Negative Width.)
   11) Check Glue logic(U604, U606) to make sure of the input/output waveforms of 8043 Clock. That is, check both 8043 Clock Input (U604 Pin3) and 8043 Clock Output (U606 Pin 1).
      (Check the minimum On/Off period of the output clock is more than 45 ㎱.)

Detailed description by each item (12 items) will be continued.

Classification	Channel Check Item	Section	FEC B'd
Items 1,2: Tuner Operating Voltage & VT Voltage			
Symptom: Locking Fails			

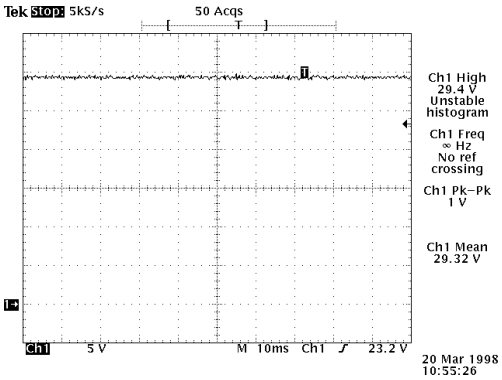
- +5V is the internal operating voltage of tuner, which causes the fluctuation of the internal frequency of tuner when Ripple or Voltage fluctuates. When the tuning voltage (30V) is abnormally low or ripple is more than 200mV, +5V causes 479.5 ㎒ IF waveform noise by being parasitic on the local frequency generated inside Tuner.

1) Tuner Operating Voltage (+5V)



- ☐ +5V is the internal operating power. Check C607 to make sure of the voltage (5.35 ~ 4.75V). Voltage failure happens mostly because U601 LM7805 fails or +7.5 is not applied to 7805 input pin. In the other cases, check the associated R,L,C devices.
- ☐ Tuner operation is sensitive to Power Ripple. So check the power ripple is within 40mVpp. Tuner operation failure happens mostly because the input voltage fluctuates or U601 LM7805 fails.

2) Tuning Voltage (30V)



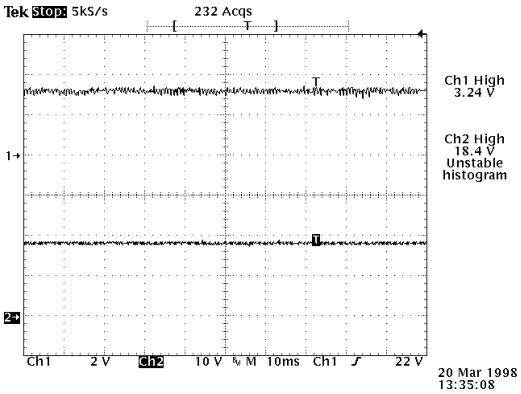
- ☐ The tuning voltage VT 30V is used to make a local OSC in Tuner. Check C40 to make sure the tuning voltage is within +28.5~ 31V. If the tuning voltage is not output, it is mostly because U800 LM317 fails. But check first C800 to make sure the input voltage is about 39V. And then replace LM317 if the resistance value of R802, R803 is correct and the state of soldering is okay.

- Countermeasure: Replace LM7805, LM317 after checking for the state of soldering and the input voltage of regulator.

Classification	Channel Check Item	Section	FEC B'd
Item 3): 13.5 / 18V LNB operating voltage fails			
Symptom: Locking Fails.			

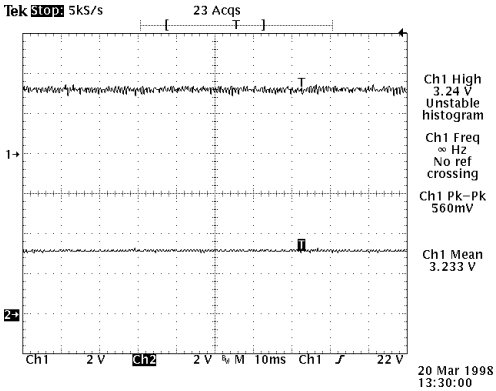
- 13.5/18V is LNB internal driving voltage, which is supplied to LNB via Tuner Loop. The voltage is used for the input power of the regulator inside LNB. In case of LNB Dual Pola, the voltage is also used when switching HOR./ VER Pola.

1) LNB Voltage (see PS B'd circuit diagram)



□ Make sure that LNB voltage is 18V or 13.5V according to the voltage of R4 POINT.
(Check C601 to make sure of HOR : 17~19V, VER: 13~14V)
If LNB voltage is not generated and H/V Control signal has no problem, check for the resistance value and the state of soldering (because the LNB voltage is determined by the resistance of R808,809, 810).

2) LNB Voltage Control Signal (see PS B'd circuit diagram)



□ CH 1: Waveform of LNB Power On/Off
When the voltage of LNB is 3V, LNB Power is turned ON. When the voltage of LNB is 0V, LNB Power is turned OFF. If LNB Power is not turned ON when the voltage of R814 is 3V, check Q801 to make sure switching works.

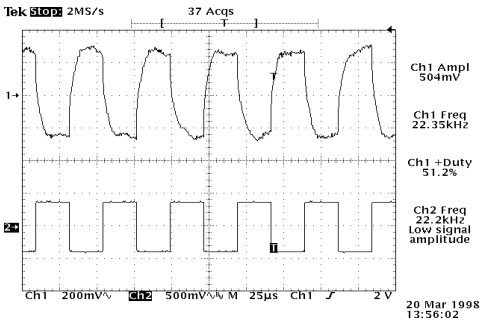
Waveform of HOR/VER Voltage Switching. When the voltage of LNB is 3.3V, 13.5V is output (R812). The switching failure mostly happens because the control voltage is not input or Q800 fails. When both control voltage and Q800 are normal, check LNB Power R812 is 3.3V and U801 Pin5 is Low.

- Countermeasure: Replace U801 LM2574-ADJ after checking for the state of soldering and the above

Classification	Channel Check Item	Section	FEC B'd
Items 4,5) 22 ㎑ Tone & Carrier Voltage			
Symptom: Locking Fails.			

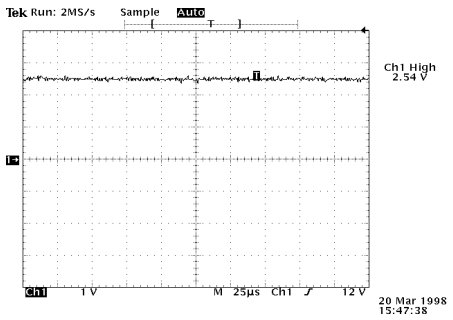
- 22 ㎑ Tone is used in Europe. It receives 950-1150 ㎒(Low Band) by loading LNB Power Supply with 22 ㎑ Tone and then selecting the local OSC inside LNB in High or Low band when the signal more than 1.2 ㎒ is input to Tuner Input because of much channel information. Carrier VCO Voltage is used as the local OSC signal to extract the final I/Q signal by generating 479.5MHz for the QPSK Demodulator inside the Tuner.

1) 22 ㎑ Tone (see Schematic Diagram page 3/36)



- ☐ Waveform of CH1: If the waveform is abnormal after checking C801 to make sure the voltage is within 400~800mV and +duty is within 45~55%, check R603 to make sure the control waveform is generated from ASIC like CH2. If the waveform is normal, check TR Q601 is switched. Otherwise, replace TR Q601.
- ☐ Defective size and cycle of waveform are mostly caused by cold soldered or non-inserted C601, R602, Q601, L601. Check with eyes.

2) Carrier VCO Voltage.



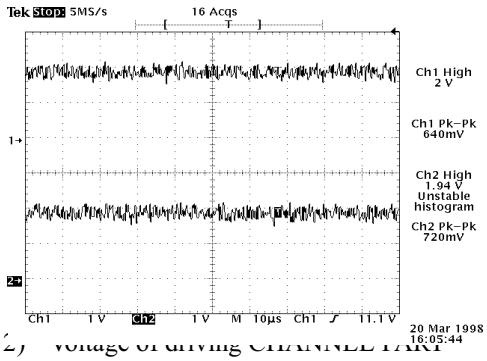
- ☐ The local VCO voltage (479.5 ㎒) is generated by setting the Carrier VCO voltage to 2.5V and then supplying it to tuner. Because 2.5V is generated by dividing +5V into R609, 610, check the voltage of U601 7805 and the resistance of R609, 610 are correct..

- Countermeasure: Replace or re-solder the transistor Q601 according to the above.

Classification	Channel Check Item	Section	FEC B'd
Items 6,7) Tuner Output I/Q & TDA 8043 Operating Voltage			
Symptom: Locking Fails			

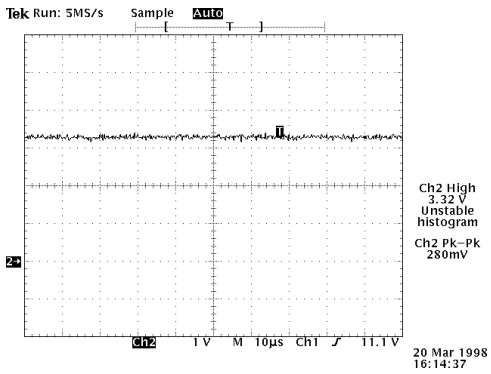
- The I/Q signal coming from Tuner Output is an analog waveform passing QPSK Demodulator inside the tuner, which is used as A/D Converter Input for the next stage. 3.3V supplied to Channel Part is divided by an inductor and used as a power supply driving TDA8043.

1) Waveform of Tuner Output I/Q



- The waveform of I/Q shows Tuner Output Signal. It is approx. 600mVpp at in 1.7V~1.9V biased by TDA 8043. So check C609, C610 to see if the waveform is as shown in the figure left. If the bias voltage is lower or not output, check for the state of soldering the power supply of TDA8043 and the devices associated to TDA8043. Check also Capacitors C609, 610 are cold soldered or unattached.

2) Voltage of driving CHANNEL PART



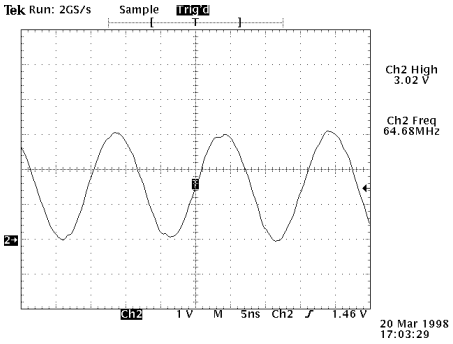
- Because 3.3V supplied to TDA 8043 passes through U53 FET, check for the state of soldering FET and PS B'd if 3.3V is not output from FET IN/OUT

Countermeasure: Check the above before doing any parts replacement. If 3.3V is shorted, it is mostly because TDA8043 fails. Therefore, check with eyes.

Classification	Channel Check Item	Section	FEC B'd
Items 8,9) TDA8043 65 ㎒ Clock & I2C Bus			
Symptom: Locking Fails			

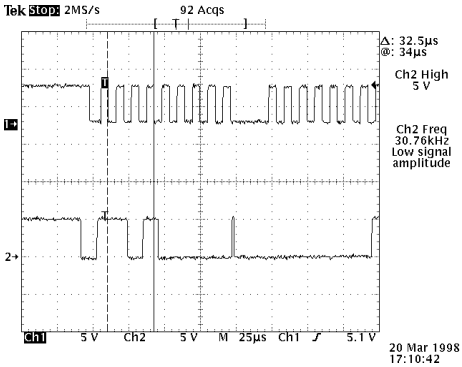
- 65 ㎒ External Clock is used by TDA8043. It makes A/D Clock using the internal divider and then it is used as an Internal Clock.
- I2C Bus is generated from ASIC separately in Tuner and TDA8043 Part. It is mainly used to set data when locking channel and to read the state of LNB.

1) 65 ㎒ Clock



- ☐ This clock (65 ㎒) is generated from Y601 X-TAL. Check R616 to see if its waveform is as shown in the figure left. If the same waveform is not provided, check C621, 622, R616 to make sure that they in themselves fail or they are cold-soldered or wrong inserted. And then replace Y601 X-TAL if they are completely okay..
- ☐ If UNLOCK happens frequently, check Y601 X-TAL using a frequency counter because X-TAL oscillation may be out of +/- 30ppm (65,001,900 ~ 64998,100 Hz)

2) Channel I2C Bus



- ☐ As shown in the waveform left, CH1 presents Clock and CH2 does a normal waveform of Data. Check TDA8043 Pin53(Data), Pin 52(Clock) to see if Data varies at Clock Pulse Negative Edge. If Timing is inappropriate, check TDA8043 Pin and I2C Bus Pin of Tuner after checking pattern
- ☐ No signal in I2C Bus Line: Mostly happens because associated pins are shorted or system is shut down. Sometimes it happens because U10 ASIC fails. Check for the value of R49, 50 (2 kΩ) of ASIC 8043 I2C Pull-up .

- Countermeasure: Re-solder (because most of failures are caused by Short or Cold Soldering).

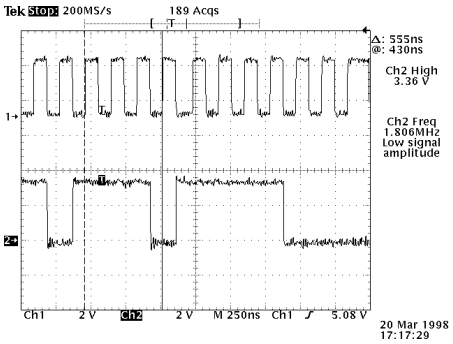
Classification	Channel Check Item	Section	FEC B'd
Items 10, 11) TDA8043 Output Signal (I)			
Symptom: Locking Fails			

- TDA8043 Output Signal is divided into TDA8043 Output Bit Clock (5.4 ㎒) , VALID(25.8 ㎑), 8Bit Data, PBAD (Low). This signal varies a little according to the set symbol rate. Each of this signal is generated when all lockings inside 8043 are fully provided.

- Locking inside TDA8043 is done in the following sequence:
  1. A/D Converter → 2. De-puncturing → 3. Viterbi Decoder
  4. De-interleaving → 5. Reed Solomon(RS) Decoder → 6 De-randomizer

- Check the state of 8043 to see if each stage is locked or not. But if TDA8043 Pins 58,57,56 (Demod Lock, Viterbi, RS) are 3.3V(High), it can be considered "locked".

1) Bit Clock & 8Bit Data



- ☐ CH1: BCLK
  It varies a little according to symbol rate.

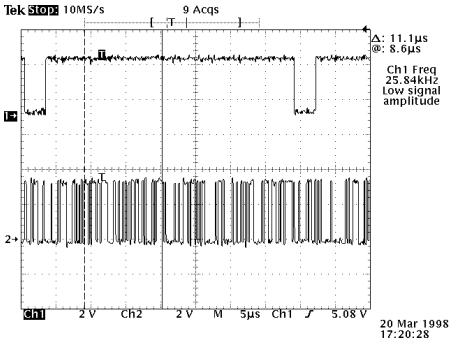
- ☐ CH2: 8Bit Data
  Data must change at Bit CLK Positive Edge.

- Bit Clock(R628) and 8BIT Data are output from 8043. Data is output after being synchronized with Bit Clock. L64108 judges the Data. If Bit Clock and Data are not output, check the items described above, re-solder TDA 8043, and than replace it. If 8043 Data is correct, but locking is not supported, check the second part of 8Bit Data Line resistor to see if it is shorted.

- Countermeasure: Prior to TDA 8043 replacement, check the state of soldering.
  Be careful with static electricity when replacing it.

Classification	Channel Check Item	Section	FEC B'd
Items 10, 11) TDA8043 Output Signal (II)			
Symptom: Locking Fails			

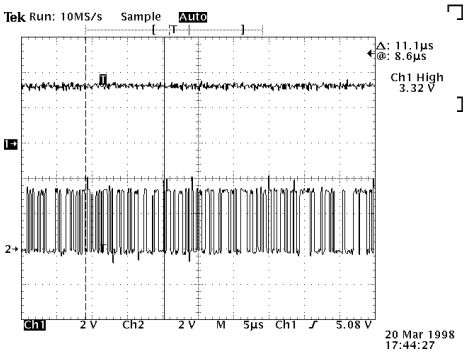
2) VALID Signal & 8Bit Data Signal



- R626 VALID Signal shows the valid section of MPEG Data.
- High section: 8bit Channel Data is available
  Low section: Parity Byte Section

- The VALID signal varies according to Symbol Rate but must be around 25.8 ㎑. If the VALID signal is not output, check the items described above and then replace TDA8043 Chip.

3) PACKET BAD Signal & 8bit DATA



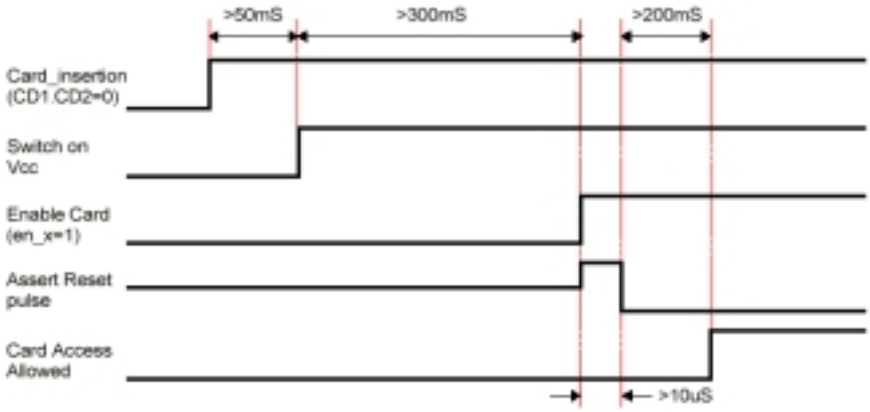
- Unlock: PBAD(Pin48) is Low. Check items 1) ~ 9) and then replace 8043
- Locking is intermittently broken: PBAD gets lower. At this time, check X-TAL 65 ㎒ oscillates within its specification. If it is okay, replace 8043.

- Countermeasure: Because TDA 8043 is easily affected by static electricity, be careful when replacing it.

Classification	Common Interface Check	Section	CPU B'd
Item: PCMCIA CI Function Check			
Symptom: Transport Stream De-scrambled by CI or Error happens when initializing CAM			

- When doing some checks relating to PCMCIA, it is necessary to understand the following sequence and follow the stream of system control.

  1) CAM Card Detection : When CAM is inserted, a signal is generated by contacting CI Slot to CD Pin .
     - C?CD1, C?CD2 signals determine the state of two CD pins. Even though the Card is disproportionally accessed, a signal is generated the moment two pins are stably accessed. (To prevent chattering, Schmitt-trigger circuit is embodied in SuperSet)
  2) CI Power Applied: Apply +5V after Card is Detected and a certain time (more than 50 ㎳) elapses.
     - Rising Time of Power must be about 300 ㎲. But if it doesn't meet the time, a problem may happen when initializing card. Therefore, be careful when checking
  3) TS Input Buffer Enable & Card Enable: Applied when about 300 ms elapses after CI power is applied
  4) CAM Reset : Applied at the same time as Card Enable. The High section must be more than 200 ㎳. For Super Set, the high section is set to about 1 sec.
  5) Card Access : Accessed when about 10 ㎲ elapses after Reset is cancelled.

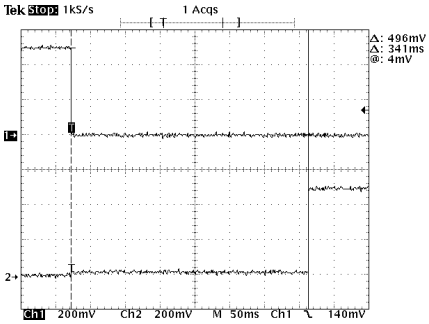


- CI Control IC is SONY CXD1957AQ, which functions as a controller of One Chip 2-Slot .

  1) CI IC Reset uses the same Reset as L64108 (Reset Signal Check)
  2) CI ACK is output to DSCK1 (U27 Pin 8) after combining with ACK of MPEG Decoder (SAA7201). Therefore, check PCMCIACS and ACK.

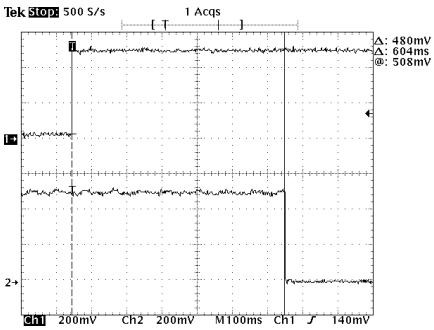
Classification	Common Interface Check	Section	CPU B'd
Item: PCMCIA Sequence Check (I)			
Symptom: Transport Stream De-scrambled by CI or Error happens when initializing CAM			

1. Card Detection & CI Power On



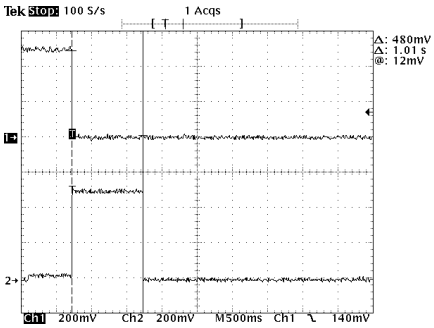
- ☐ CH 1 shows Card Detection Signal. Check U27 Pins 6, 11.
- ☐ CH 2 shows CI Power. Check JP 6, 7 Pins 17, 18, 51, 52. CI Power must be applied when at least 50 ㎳ elapses after CD signal is generated. After the CD signal is generated, check the level of power signal is about 0V.

2.



- ☐ CH 1 shows CI Power On Signal.
- ☐ CH 2 shows Card Enable & TS Input Buffer Enable Signal. It must be applied when about 300 ms elapses after applying power. If timing is out of line with the mentioned one, Latch-Up may happen.

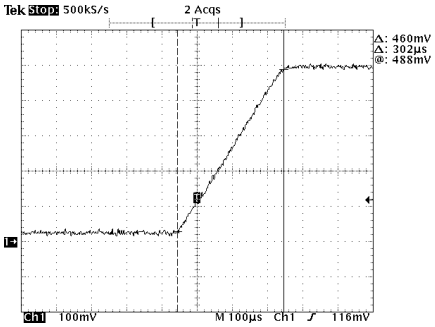
3.



- ☐ CH 1shows Card Enable Signal
- ☐ CH 2 shows Card Reset Signal. It is applied at almost same time as Card Enable. The High section must be more than 10 ㎲. For Super Set, the high section is set to about 1 sec.

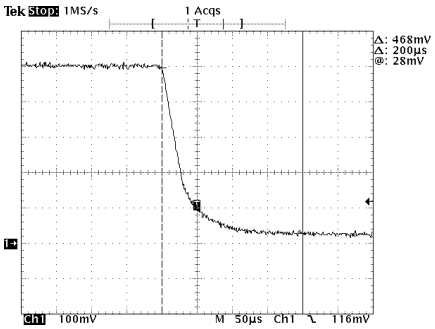
Classification	Common Interface Check	Section	CPU B'd
Item: PCMCIA Sequence Check (II)			
Symptom: Transport Stream De-scrambled by CI or Error happens when initializing CAM			

4. CI Power Rising Time Check



- ☐ Measurement Waveform of CI Power Rising Time. It must be about 300 μs.
- ☐ If any abnormal rising time is measured, check CI Power, in case of U18(IRF7303) and Slot1, R110, C120, C125, Q6, R111, R108 are not inserted or properly soldered. Also in case of Slot 2, check associated parts (see Schematic Diagram)

5. CI Power Falling Time Check



- ☐ Measurement Waveform of CI Power Falling Time
- ☐ 3~300 ms: Provided in PCMCIA Specification Just refer to it (because there is no possibility that this will be a problem).

- PCMCIA Sequence Control signals are defined as follows. (See Schematic Diagram)

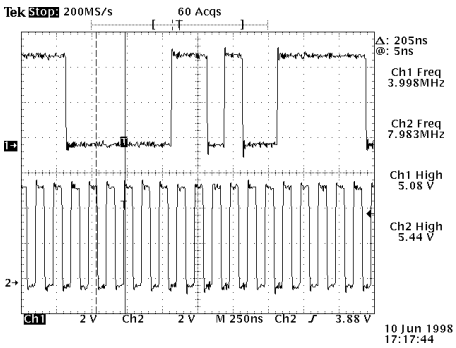
1. CAS1SIG, CAS2SIG : Enables TS Stream Input using CAM (Active low)
2. CAS1CD, CAS2CD : Transmits CAM Insert Signal to CI Control IC (Active Low)
3. CAS1RST,CAS2RST : CAM Reset (Active High)
4. CAS1PWR,CAS2PWR : CAM Power Control (Active Low)
5. CAS1CS, CAS2CS : Selects CAM 1 and CAM2 g(Active Low)
6. CAS1MUX,CAS2MUX : Low = 8043 Data Output, High = CAM 1 De-scramble TS Output
7. IORD, IOWR : Card Memory R/W (Active Low)
8. WE, OE : Card I/O R/W (Active Low)

Classification	Common Interface Check	Section	CPU B'd
Item: CAM Stream Input & Output.			
Symptom: Locking Fails & Tessellated (mosaic) screen, CAM Operation Fails			

- The CAM Control Logic functions only for the channel which is de-scrambled by CAM. Therefore, Free Channel is not input to CAM but it is simply switched (Buffer : 74HC257 U19~23, 31~34) and then input to L64108 (MUX & CPU).

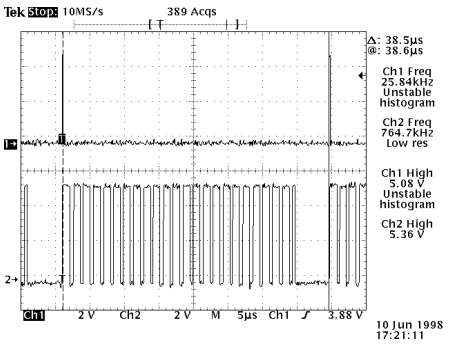
- In case of Scramble Channel, CAS1CD, CAS2CD (Active Low) are generated after CAM is inserted. CAM is reset (Active High) after power is supplied by U18 FET. And TS stream is supplied by Buffer Control (U19, 20). De-scrambling is performed after initializing CAM (CIR Reading, COR Writing).

1) CAM Input & Output Stream (I)



- ☐ When CAM is inserted to Slot 1, check TS Data is output from U19.
- ☐ When CAM is inserted to Slot 2, check TS Data is output from U31
- ☐ If TS Data is not output, check U19, 31 Buffer or Gate Pins 1,19 are not Low.
- ☐ As shown in the figure left, Ch1 shows the waveform of TS and Ch2 shows Clock (U20,Pin 6).

2) CAM Input & Output Stream(II)

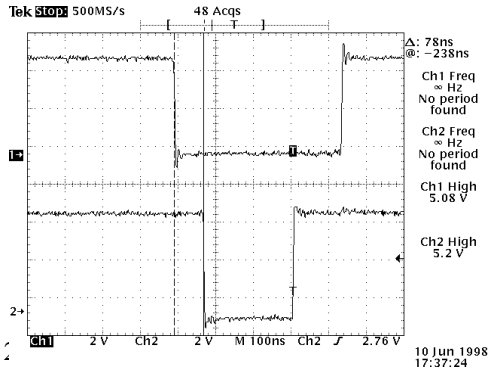


- ☐ When CAM is inserted to Slot 1,2, check CLK, VLD, STR are output from U20. (Compare with the waveform shown in the figure left.)
- ☐ As shown in the figure left, Ch1 shows the waveform of STR and Ch2 shows VLD. Check each signal is within Clock Duty 48~52.
- ☐ Check TS Data output from CAM and CLK,VLD, STR are input to 74HC257(U21~23, 32~34).
- ☐ CAM 1 is low if Gate Control passes by CAM. Therefore, check the input/output of 74HC257 (Same as CAM 2).

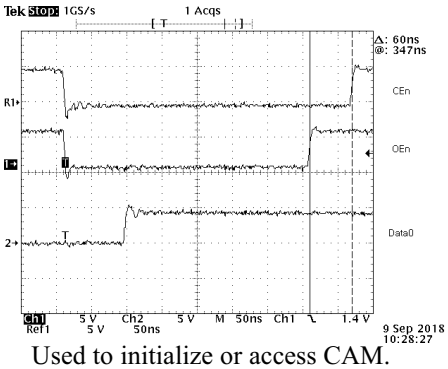
Classification	Common Interface Check	Section	CPU B'd
Item: CI-CAM Control Signal			
Symptom: Locking Fails & CAM Operation Fails			

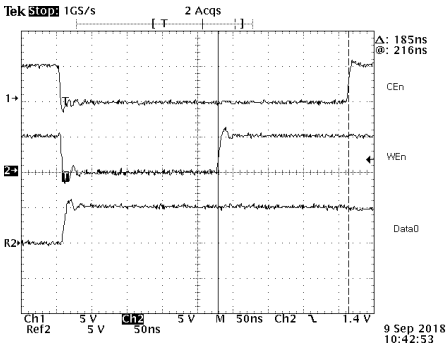
- Problems relating to de-scrambling are caused by CAM Card I/O and Memory Access. Therefore, refer to the following waveforms when troubleshooting CAM operation failure.

1) CAM CS & IORD, IOWR



Used to initialize or access CAM.
Check JP5, 6 Pins 7, 44, 45 to see if the waveform as shown in the figure left is output.
CH1shows CAS1CS, CAS2CS and CH2 shows IORD, IOWR.
If the waveform as shown in the figure left is not output, replace CAM.





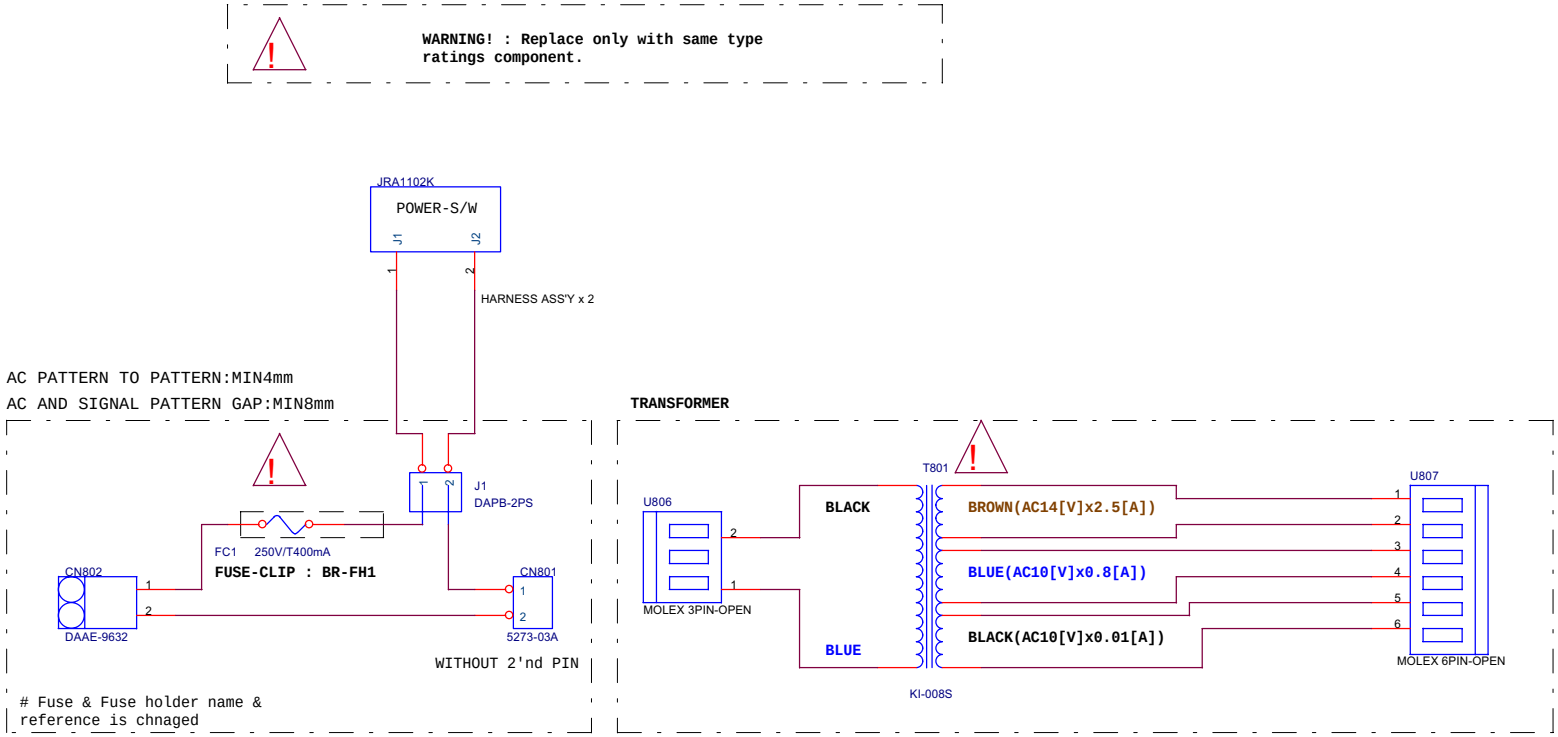
- Used to initialize or access CAM.
  Check the signal pin of CI Slot to see if the waveforms as shown in the figure above are output.
  - ✓ CH1: CAS1CS, CAS2CS signal
  - ✓ CH2: OE n, Wen signal
  - ✓ CH3: CI Data 0 signal

If the waveforms as shown in the figure above are not output, replace CAM or check CI Control IC is accessed. That is, check PCMCIACS (U26 Pin 14) and DSACK1 (U27 Pin 3).

SuperSet Schematic Diagram

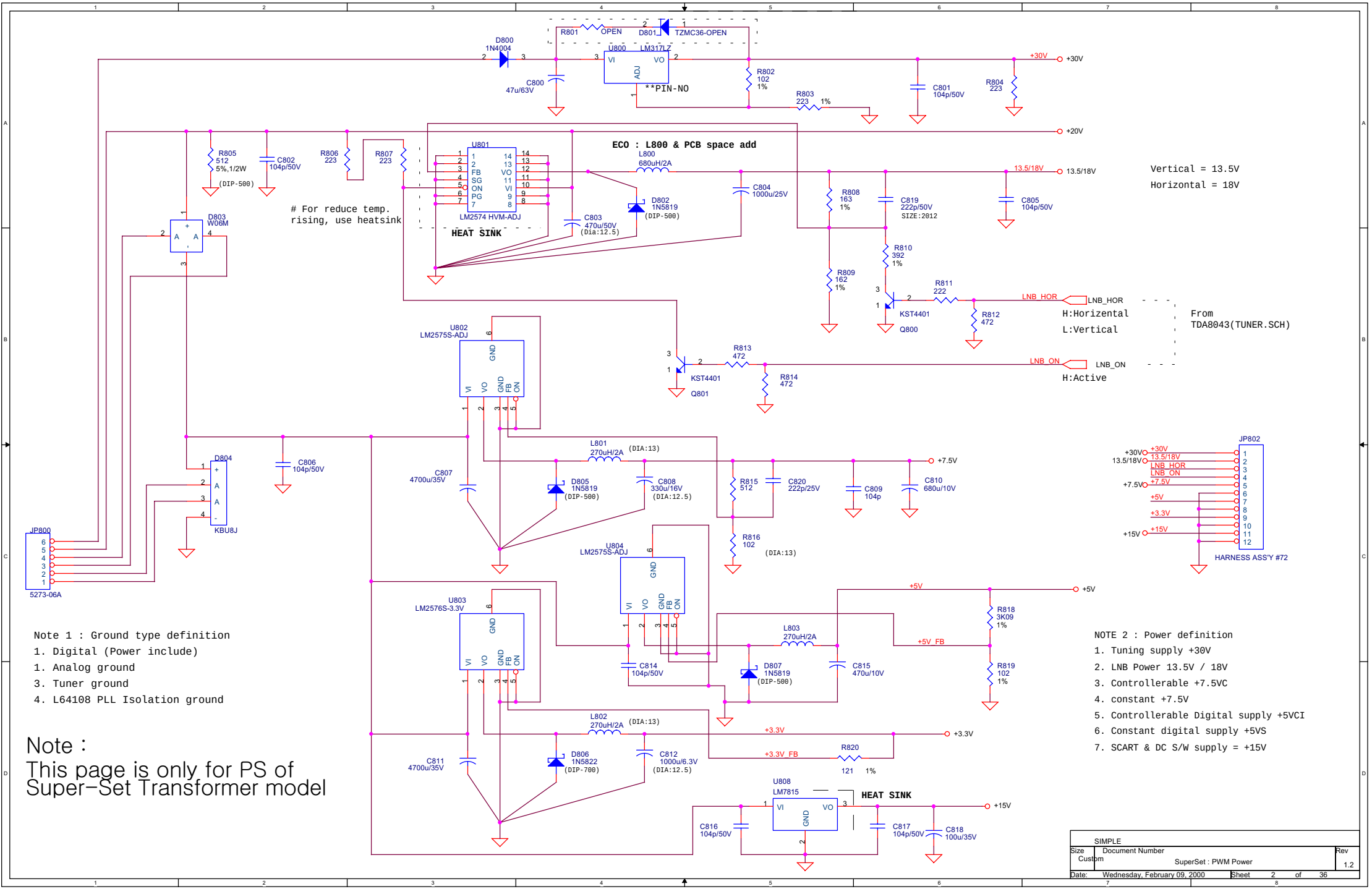
- **CPU Board Rev 1.5 , 2.0 and 2.1**
- **FEC Board Rev 1.1 , 1.2**
- **FRONT Board Rev 1.0**
- **SMART CARD Board Rev 1.0**

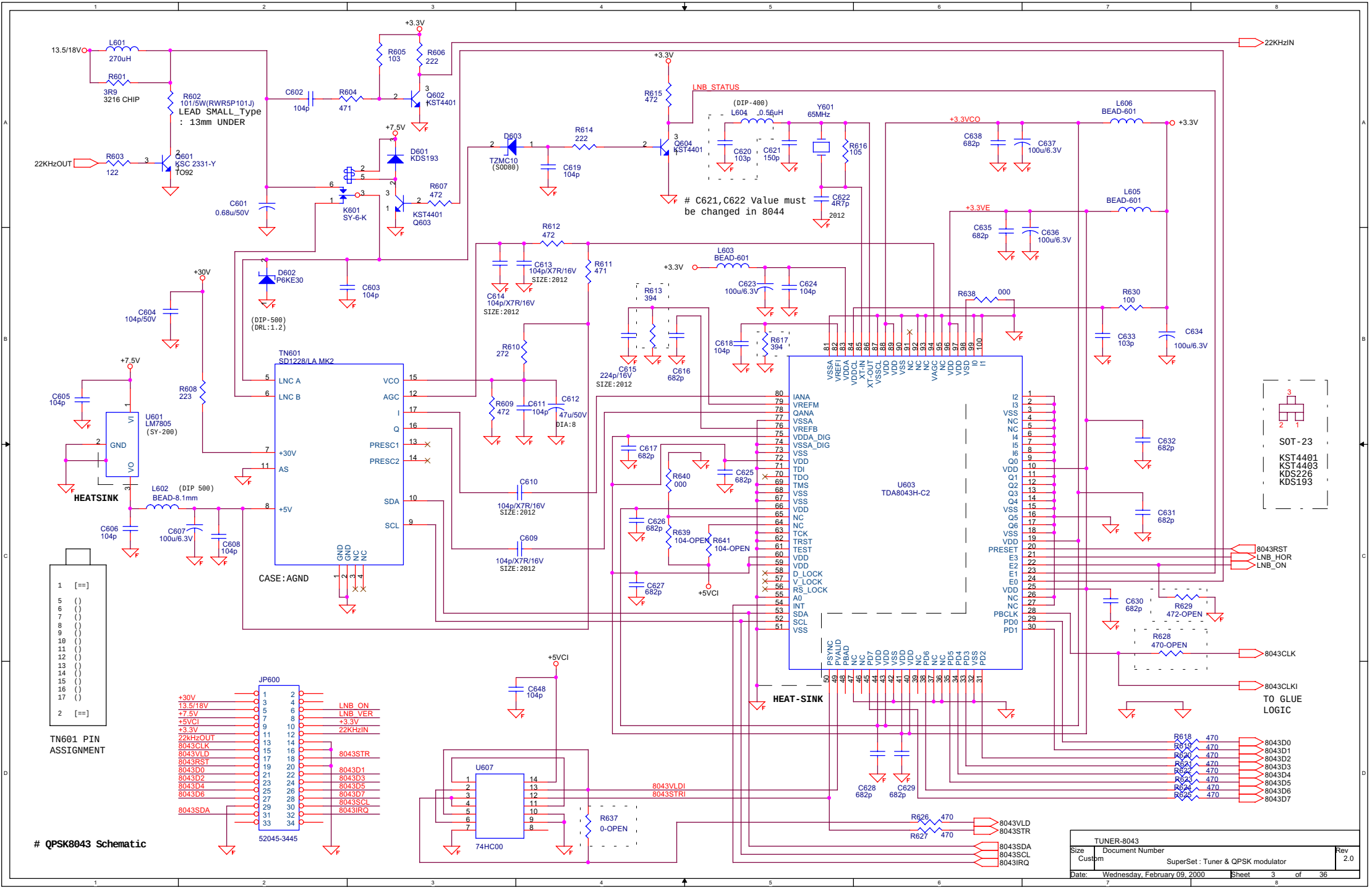
Note :
This page is only for PS of Super-Set Transformer model

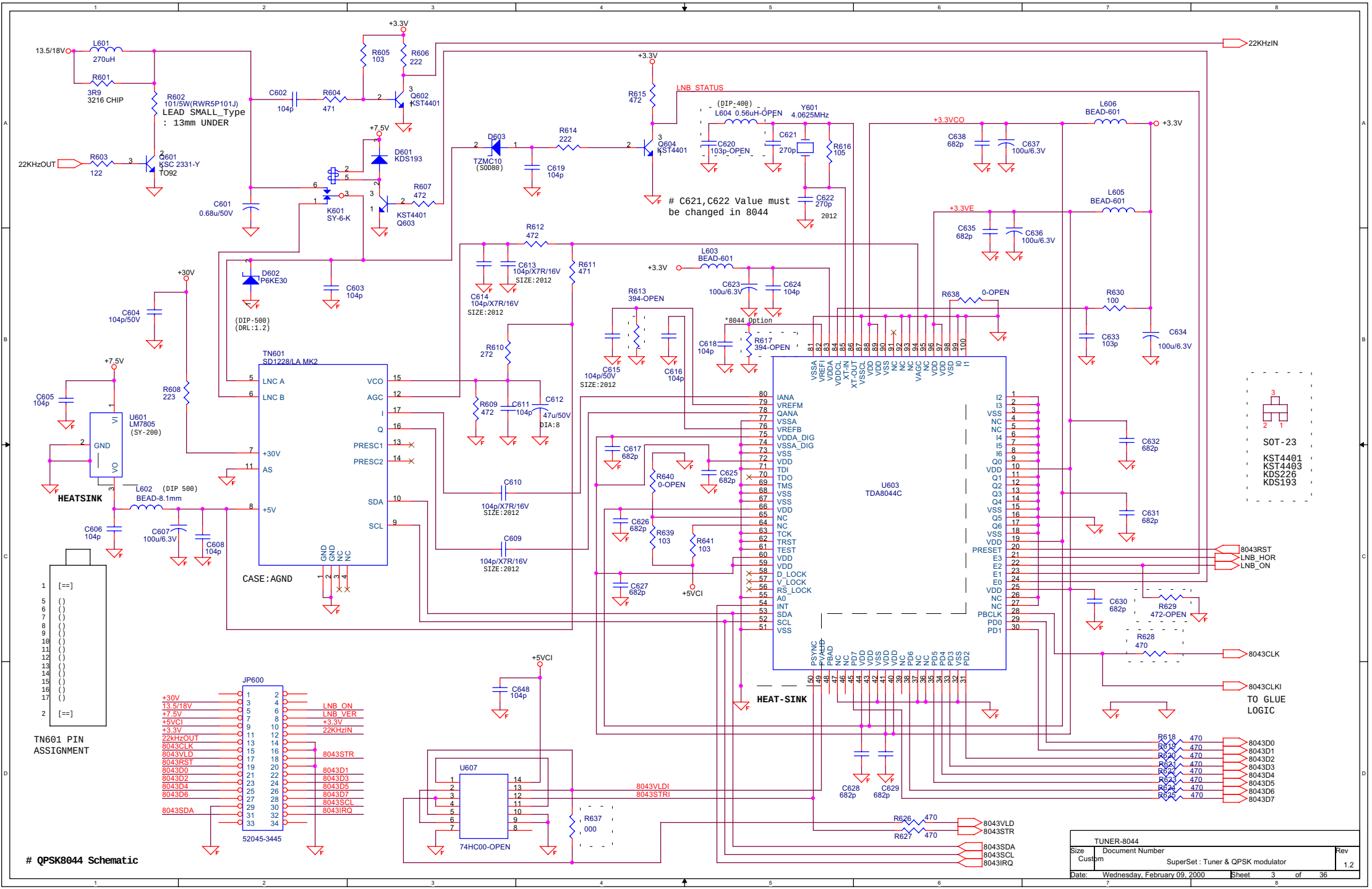


Note : Sub-b'd is to be summed with power b'd

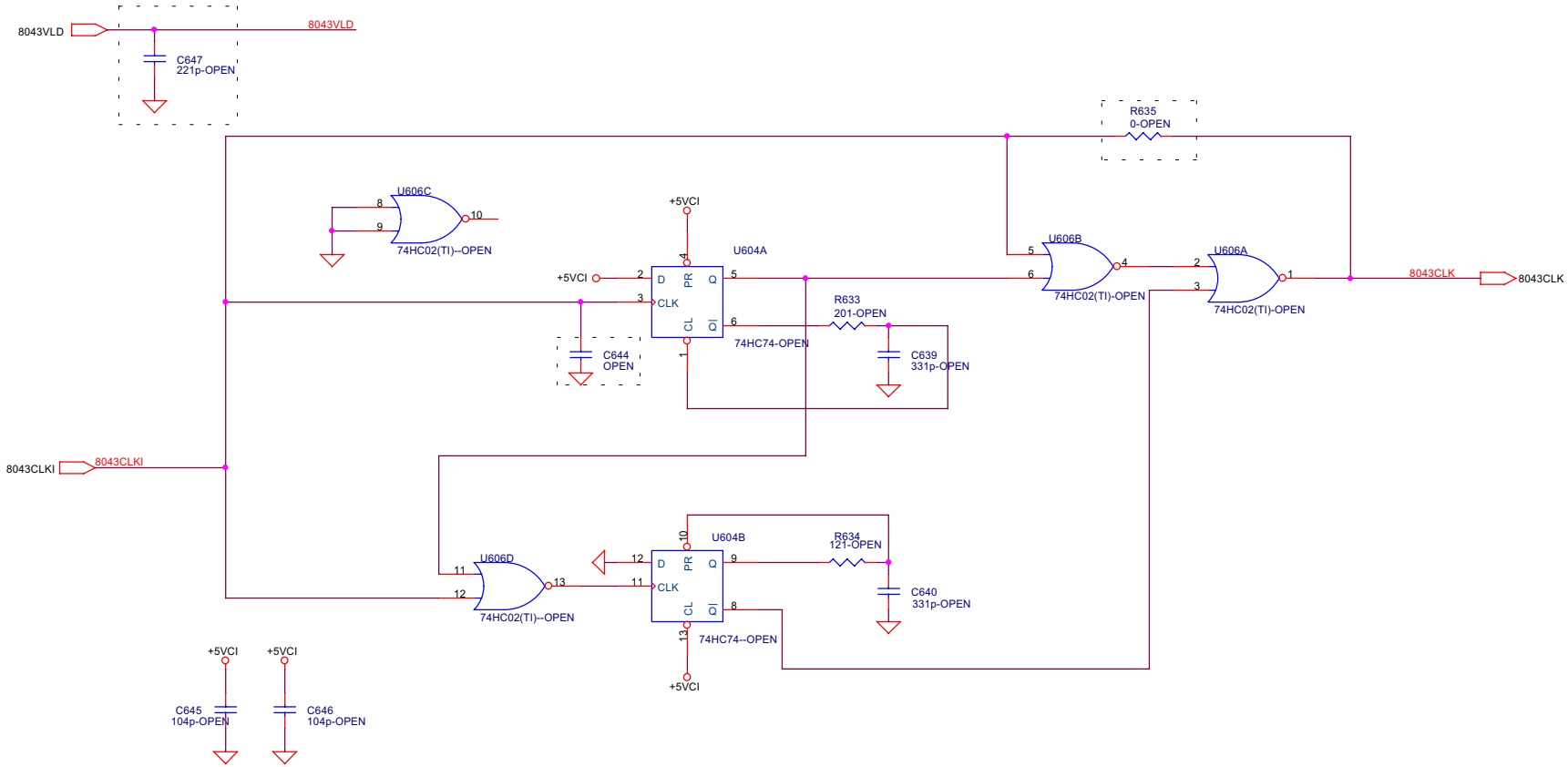
TRANS		
Size Custom	Document Number SuperSet : Back-panel & Transformer	Rev 1.2
Date: Wednesday, February 09, 2000	Sheet 1 of 36	


R801 OPEN
D801 TZMC36-OPEN
D800 1N4004
U800 LM317LZ
VI VO ADJ
**PIN-NO
C800 47u/63V
R802 102 1%
R803 223 1%
C801 104p/50V
R804 223
+30V
+20V
R805 512 5%,1/2W (DIP-500)
C802 104p/50V
R806 223
R807 223
U801
LM2574 HVM-ADJ
FB SG ON PG VO VI
HEAT SINK
ECO : L800 & PCB space add
L800 680uH/2A
D802 1N5819 (DIP-500)
C803 470u/50V (Dia:12.5)
C804 1000u/25V
R808 163 1%
C819 222p/50V SIZE:2012
C805 104p/50V
13.5/18V
Vertical = 13.5V
Horizontal = 18V
# For reduce temp. rising, use heatsink
D803 W06M
R809 162 1%
R810 392 1%
R811 222
KST4401 Q800
R812 472
LNB_HOR
H:Horizental
L:Vertical
From TDA8043(TUNER.SCH)
U802 LM2575S-ADJ
GND VI VO GND FB ON
R813 472
KST4401 Q801
R814 472
LNB_ON
H:Active
L801 270uH/2A (DIA:13)
+7.5V
D804 KBU8J
C806 104p/50V
C807 4700u/35V
D805 1N5819 (DIP-500)
C808 330u/16V (DIA:12.5)
R815 512
C820 222p/25V
C809 104p
C810 680u/10V
R816 102 (DIA:13)
JP800 5273-06A
U804 LM2575S-ADJ
JP802 HARNESS ASS'Y #72
+30V 13.5/18V LNB_HOR LNB_ON +7.5V +5V +3.3V +15V
U803 LM2576S-3.3V
+5V
R818 3K09 1%
L803 270uH/2A
+5V_FB
C814 104p/50V
D807 1N5819 (DIP-500)
C815 470u/10V
R819 102 1%
L802 270uH/2A (DIA:13)
+3.3V
+3.3V_FB
R820 121 1%
C811 4700u/35V
D806 1N5822 (DIP-700)
C812 1000u/6.3V (DIA:12.5)
U808 LM7815
VI VO GND
HEAT SINK
+15V
C816 104p/50V
C817 104p/50V
C818 100u/35V
Note 1 : Ground type definition
1. Digital (Power include)
1. Analog ground
3. Tuner ground
4. L64108 PLL Isolation ground
Note :
This page is only for PS of Super-Set Transformer model
NOTE 2 : Power definition
1. Tuning supply +30V
2. LNB Power 13.5V / 18V
3. Controllable +7.5VC
4. constant +7.5V
5. Controllable Digital supply +5VCI
6. Constant digital supply +5VS
7. SCART & DC S/W supply = +15V
SIMPLE
Size Custom
Document Number
SuperSet : PWM Power
Rev 1.2
Date: Wednesday, February 09, 2000
Sheet 2 of 36

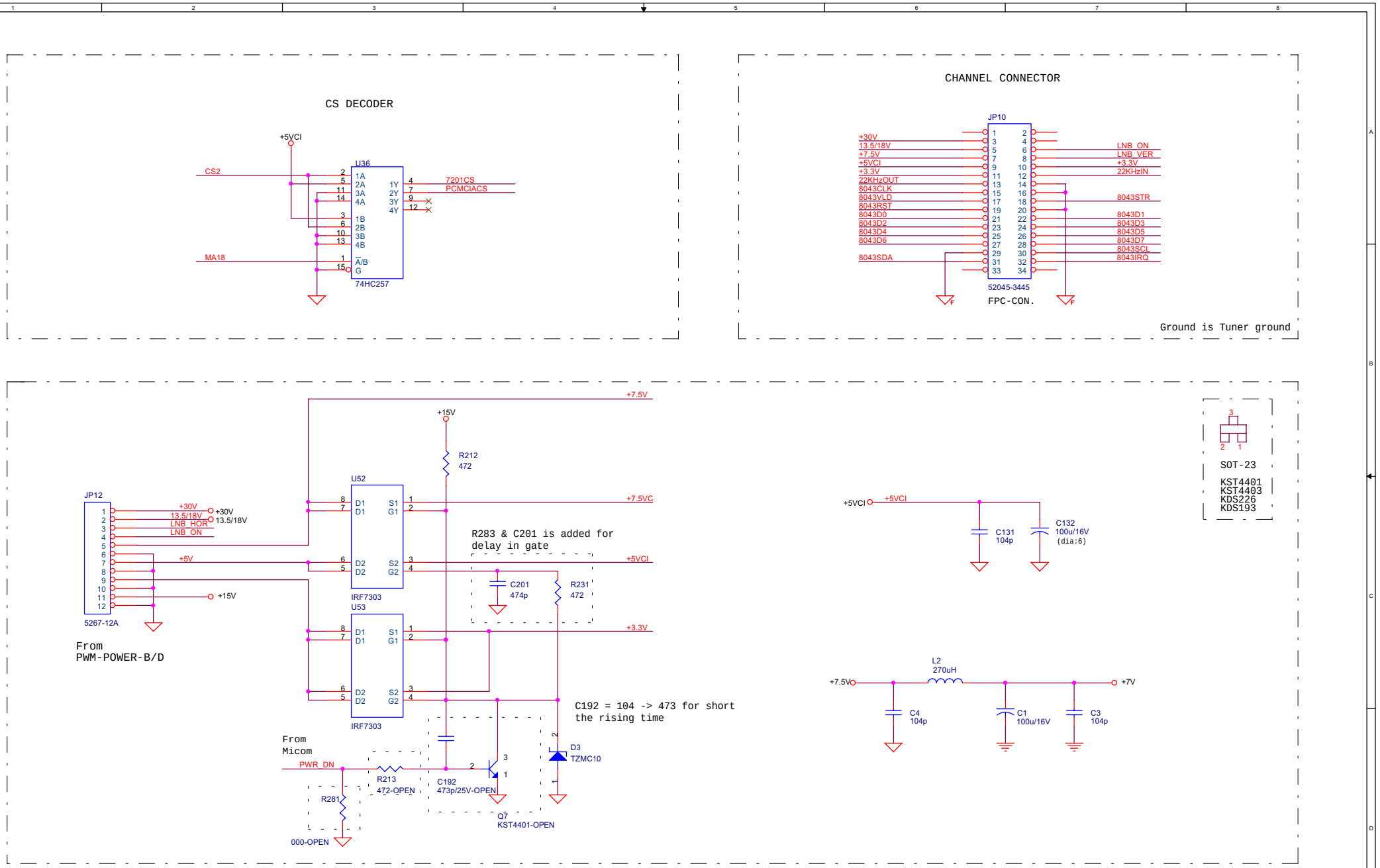

13.5/18V
L601
270uH
R601
3R9
3216 CHIP
R602
101/5W(RWR5P101J)
LEAD SMALL_Type
: 13mm UNDER
22KHzOUT
R603
122
Q601
KSC 2331-Y
TO92
C601
0.68u/50V
C602
104p
R604
471
R605
103
R606
222
+3.3V
Q602
KST4401
+7.5V
D601
KDS193
K601
SY-6-K
R607
472
KST4401
Q603
D603
TZMC10
(SOD80)
C619
104p
R614
222
Q604
KST4401
R615
472
LNB_STATUS
(DIP-400)
L604 0.56uH
C620
103p
C621
150p
Y601
65MHz
R616
105
C622
4R7p
2012
C621,C622 Value must
be changed in 8044
+3.3VCO
C638
682p
C637
100u/6.3V
L606
BEAD-601
+3.3V
22KHzIN
+3.3VE
C635
682p
C636
100u/6.3V
L605
BEAD-601
R612
472
C613
104p/X7R/16V
SIZE:2012
C614
104p/X7R/16V
SIZE:2012
R611
471
L603
BEAD-601
C623
100u/6.3V
C624
104p
R613
394
C615
224p/16V
SIZE:2012
C616
682p
C618
104p
R617
394
R638
000
R630
100
C633
103p
C634
100u/6.3V
+30V
D602
P6KE30
(DIP-500)
(DRL:1.2)
C603
104p
C604
104p/50V
R610
272
R609
472
C611
104p
C612
47u/50V
DIA:8
TN601
SD1228/LA MK2
LNC A
LNC B
+30V
AS
+5V
VCO
AGC
I
Q
PRESC1
PRESC2
SDA
SCL
GND
GND
NC
NC
CASE:AGND
C605
104p
U601
LM7805
(SY-200)
VI
GND
VO
HEATSINK
R608
223
L602 (DIP 500)
BEAD-8.1mm
C606
104p
C607
100u/6.3V
C608
104p
C610
104p/X7R/16V
SIZE:2012
C609
104p/X7R/16V
SIZE:2012
C617
682p
R640
000
C625
682p
C626
682p
R639
104-OPEN
R641
104-OPEN
C627
682p
+5VCI
U603
TDA8043H-C2
IANA
VREFM
QANA
VSSA
VREFB
VDDA_DIG
VSSA_DIG
VSS
VDD
TDI
TDO
TMS
VSS
VSS
VDD
NC
NC
TCK
TRST
TEST
VDD
VDD
D_LOCK
V_LOCK
RS_LOCK
A0
INT
SDA
SCL
VSS
PRESET
E3
E2
E1
E0
PBCLK
PD0
PD1
PSYNC
PVALID
PBAD
C632
682p
C631
682p
C630
682p
R629
472-OPEN
R628
470-OPEN
8043RST
LNB_HOR
LNB_ON
8043CLK
8043CLKI
TO GLUE
LOGIC
SOT-23
KST4401
KST4403
KDS226
KDS193
HEAT-SINK
C648
104p
JP600
52045-3445
+30V
13.5/18V
+7.5V
+5VCI
+3.3V
22KHzOUT
8043CLK
8043RST
8043D0
8043D2
8043D4
8043D6
8043SDA
LNB_ON
LNB_VER
+3.3V
22KHzIN
8043STR
8043D1
8043D3
8043D5
8043D7
8043SCL
8043IRQ
U607
74HC00
8043VLDI
8043STRI
R637
0-OPEN
C628
682p
C629
682p
R618
R619
R620
R621
R622
R623
R624
R625
470
8043D0
8043D1
8043D2
8043D3
8043D4
8043D5
8043D6
8043D7
R626
R627
8043VLD
8043STR
8043SDA
8043SCL
8043IRQ
TN601 PIN
ASSIGNMENT
QPSK8043 Schematic
TUNER-8043
Size
Custom
Document Number
SuperSet : Tuner & QPSK modulator
Rev
2.0
Date: Wednesday, February 09, 2000
Sheet 3 of 36


13.5/18V
L601
270uH
R601
3R9
3216 CHIP
R602
101/5W(RWR5P101J)
LEAD SMALL_Type
: 13mm UNDER
22KHzOUT
R603
122
Q601
KSC 2331-Y
TO92
C601
0.68u/50V
C602
104p
R604
471
R605
103
R606
222
Q602
KST4401
+3.3V
+7.5V
D601
KDS193
K601
SY-6-K
R607
472
KST4401
Q603
D603
TZMC10
(SOD80)
C619
104p
R614
222
Q604
KST4401
R615
472
LNB_STATUS
(DIP-400)
L604 0.56uH-OPEN
C620
103p-OPEN
Y601
4.0625MHz
C621
270p
R616
105
C622
270p
2012
C621,C622 Value must
be changed in 8044
+3.3VCO
C638
682p
C637
100u/6.3V
L606
BEAD-601
+3.3V
22KHzIN
+3.3VE
C635
682p
C636
100u/6.3V
L605
BEAD-601
R612
472
R611
471
C613
104p/X7R/16V
SIZE:2012
C614
104p/X7R/16V
SIZE:2012
L603
BEAD-601
C623
100u/6.3V
C624
104p
R613
394-OPEN
C615
104p/50V
SIZE:2012
C616
104p
C618
104p
*8044 Option
R617
394-OPEN
R638
0-OPEN
R630
100
C633
103p
C634
100u/6.3V
+30V
C604
104p/50V
D602
P6KE30
(DIP-500)
(DRL:1.2)
C603
104p
R610
272
R609
472
C611
104p
C612
47u/50V
DIA:8
C610
104p/X7R/16V
SIZE:2012
C609
104p/X7R/16V
SIZE:2012
TN601
SD1228/LA MK2
LNC A
LNC B
+30V
AS
+5V
VCO
AGC
I
Q
PRESC1
PRESC2
SDA
SCL
GND
GND
NC
NC
CASE:AGND
+7.5V
C605
104p
U601
LM7805
(SY-200)
VI
GND
VO
HEATSINK
L602 (DIP 500)
BEAD-8.1mm
C606
104p
C607
100u/6.3V
C608
104p
R608
223
U603
TDA8044C
IANA
VREFM
QANA
VSSA
VREFB
VDDA_DIG
VSSA_DIG
VSS
VDD
TDI
TDO
TMS
VSS
VSS
VDD
NC
NC
TCK
TRST
TEST
VDD
VDD
D_LOCK
V_LOCK
RS_LOCK
A0
INT
SDA
SCL
VSS
PSYNC
PVALID
PBAD
PD7
PD6
PD5
PD4
PD3
PD2
I2
I3
I4
I5
I6
Q0
Q1
Q2
Q3
Q4
Q5
Q6
PRESET
E3
E2
E1
E0
PBCLK
PD0
PD1
C617
682p
R640
0-OPEN
C625
682p
C626
682p
R639
103
R641
103
C627
682p
+5VCI
C632
682p
C631
682p
C630
682p
R629
472-OPEN
R628
470
8043RST
LNB_HOR
LNB_ON
8043CLK
8043CLKI
TO GLUE
LOGIC
SOT-23
KST4401
KST4403
KDS226
KDS193
HEAT-SINK
C648
104p
R618
R619
R620
R621
R622
R623
R624
R625
470
8043D0
8043D1
8043D2
8043D3
8043D4
8043D5
8043D6
8043D7
C628
682p
C629
682p
R626
R627
8043VLD
8043STR
8043SDA
8043SCL
8043IRQ
JP600
+30V
13.5/18V
+7.5V
+5VCI
+3.3V
22kHzOUT
8043CLK
8043VLD
8043RST
8043D0
8043D2
8043D4
8043D6
8043SDA
LNB_ON
LNB_VER
+3.3V
22KHzIN
8043STR
8043D1
8043D3
8043D5
8043D7
8043SCL
8043IRQ
52045-3445
U607
8043VLDI
8043STRI
R637
000
74HC00-OPEN
TN601 PIN
ASSIGNMENT
QPSK8044 Schematic
TUNER-8044
Size
Custom
Document Number
SuperSet : Tuner & QPSK modulator
Rev
1.2
Date: Wednesday, February 09, 2000
Sheet 3 of 36

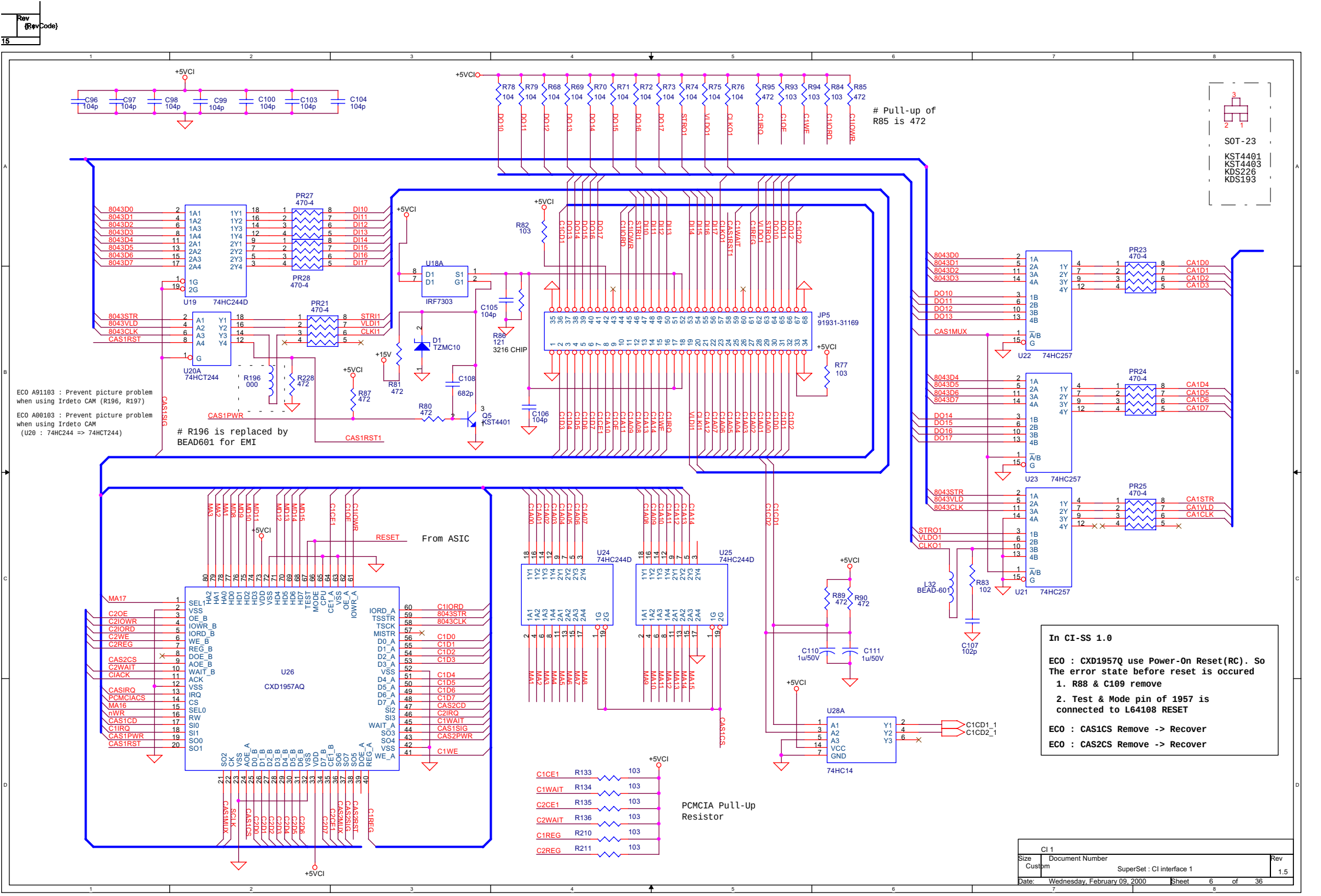
Note :
This page is only for TDA8043

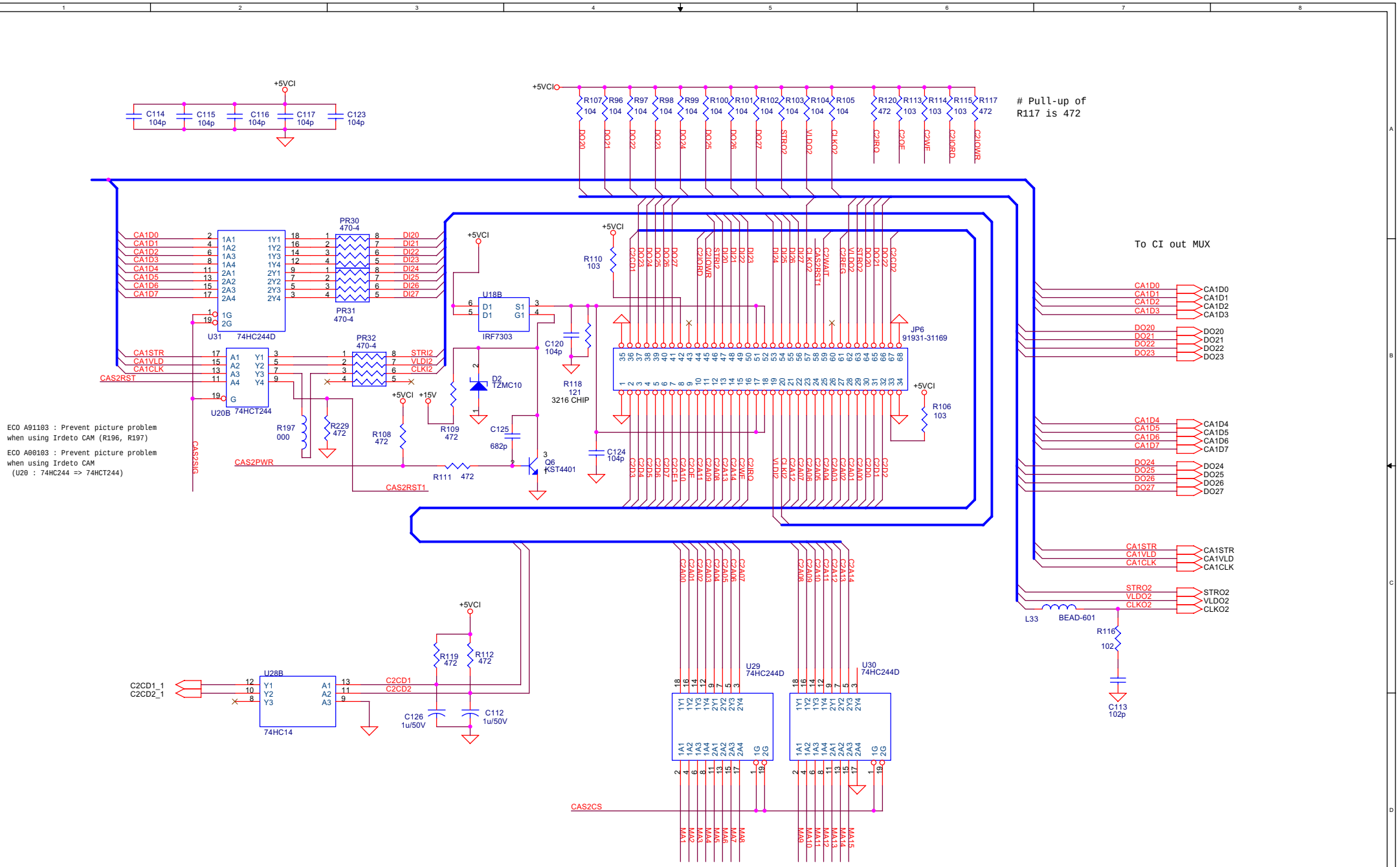


GLUE43		
Size Custom	Document Number SuperSet : Glue logic for 8043 CLK	Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 4 of 36	



CONNECT0		
Size: Custom	Document Number: SuperSet : Main External connector	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 5 of 36	

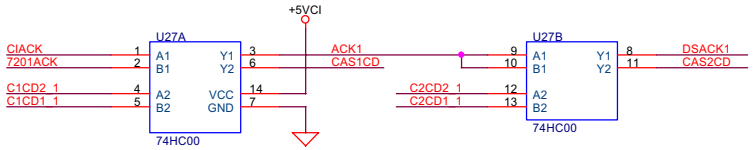

Rev
{RevCode}
15
+5VCI
C96 104p
C97 104p
C98 104p
C99 104p
C100 104p
C103 104p
C104 104p
R78 104
R79 104
R68 104
R69 104
R70 104
R71 104
R72 104
R73 104
R74 104
R75 104
R76 104
R95 472
R93 103
R94 103
R84 103
R85 472
Pull-up of
R85 is 472
SOT-23
KST4401
KST4403
KDS226
KDS193
U19 74HC244D
PR27 470-4
PR28 470-4
PR21 470-4
U20A 74HCT244
R196 000
R228 472
R87 472
R81 472
R80 472
U18A
IRF7303
D1 TZMC10
C105 104p
R86 121 3216 CHIP
C108 682p
Q5 KST4401
C106 104p
R82 103
JP5 91931-31169
R77 103
ECO A91103 : Prevent picture problem
when using Irdeto CAM (R196, R197)
ECO A00103 : Prevent picture problem
when using Irdeto CAM
(U20 : 74HC244 => 74HCT244)
R196 is replaced by
BEAD601 for EMI
U22 74HC257
U23 74HC257
U21 74HC257
PR23 470-4
PR24 470-4
PR25 470-4
L32 BEAD-601
R83 102
C107 102p
U26
CXD1957AQ
From ASIC
U24 74HC244D
U25 74HC244D
R89 472
R90 472
C110 1u/50V
C111 1u/50V
U28A
74HC14
C1CD1_1
C1CD2_1
R133 103
R134 103
R135 103
R136 103
R210 103
R211 103
PCMCIA Pull-Up
Resistor
In CI-SS 1.0
ECO : CXD1957Q use Power-On Reset(RC). So
The error state before reset is occured
1. R88 & C109 remove
2. Test & Mode pin of 1957 is
connected to L64108 RESET
ECO : CAS1CS Remove -> Recover
ECO : CAS2CS Remove -> Recover
CI 1
Size Custom
Document Number
SuperSet : CI interface 1
Rev 1.5
Date: Wednesday, February 09, 2000
Sheet 6 of 36



CI 2			
Size: Custom	Document Number: SuperSet : CI interface 2		Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 7 of 36		

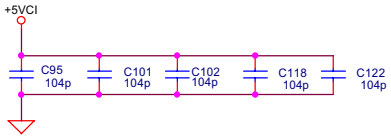
xde}

ACK signal generator



L64108 Pull-Up

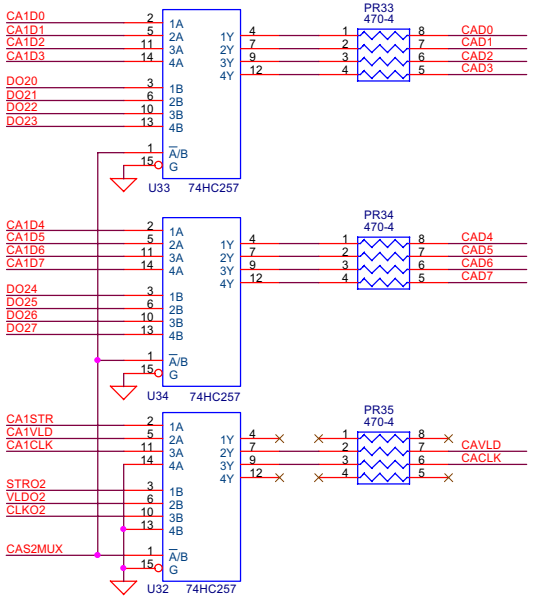
This pull is important for CPU operation



CI output Interface

From CI 2 Interface

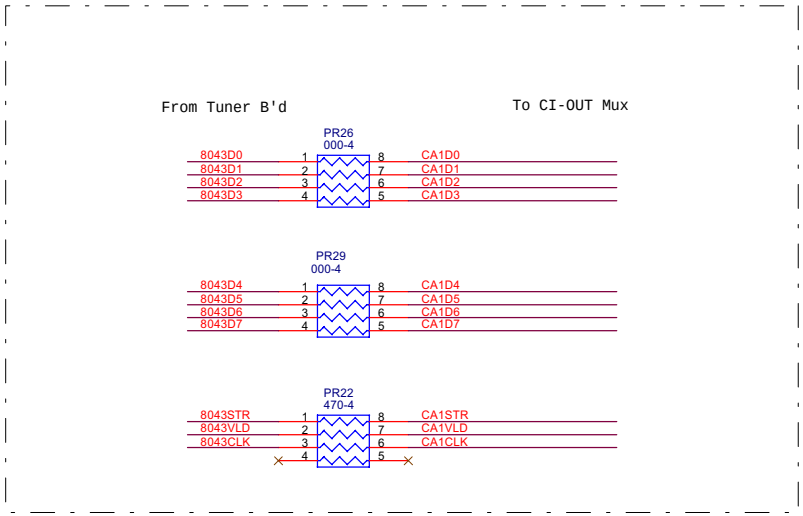
To L64108



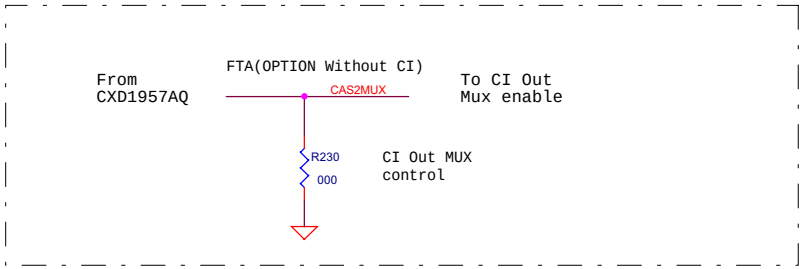
 # This part is needed in all model for TS current

CI-OUT			
Size: Custom	Document Number: SuperSet : CI out interface		Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 8 of 36		

TS 1 interface

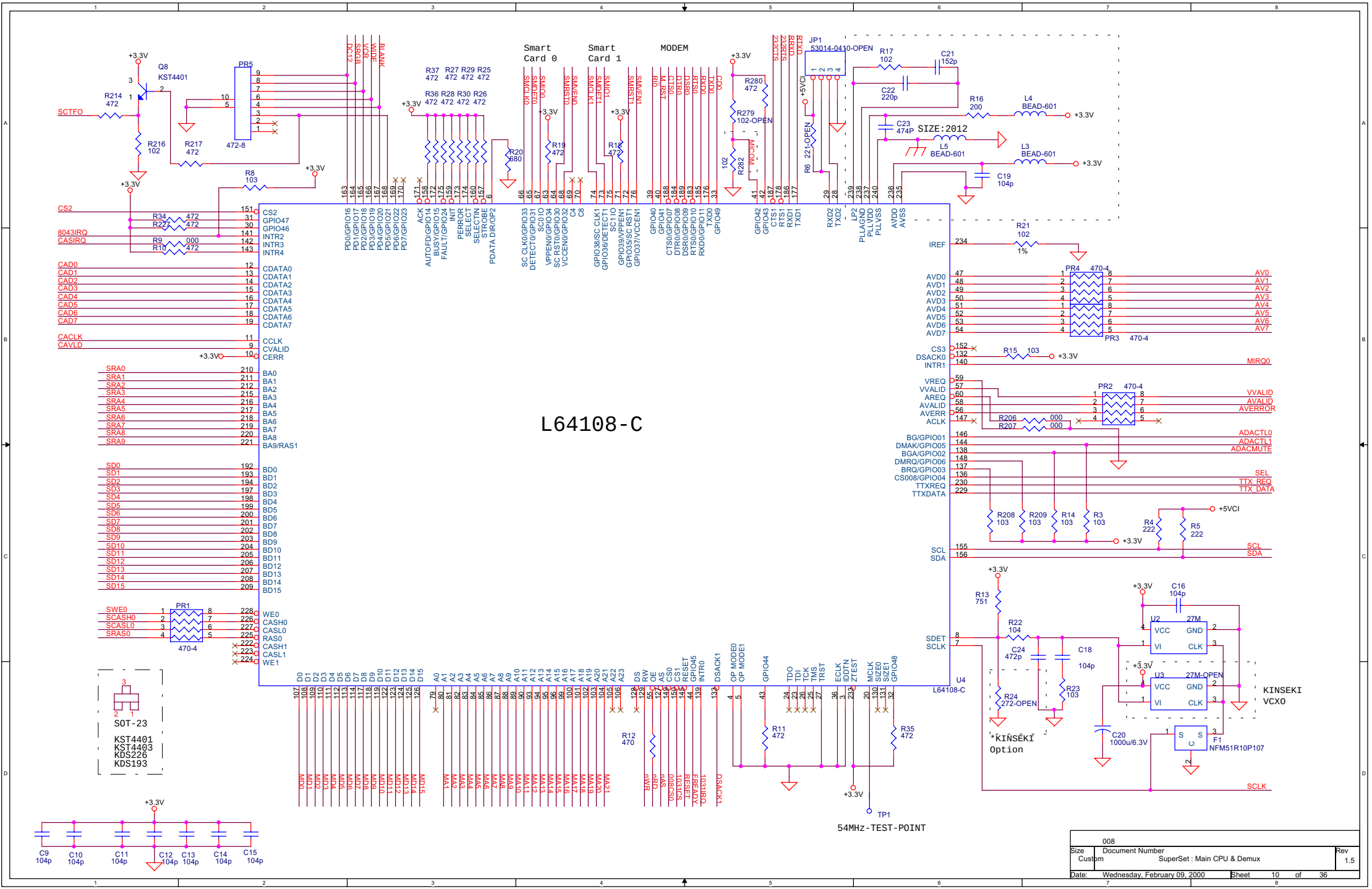


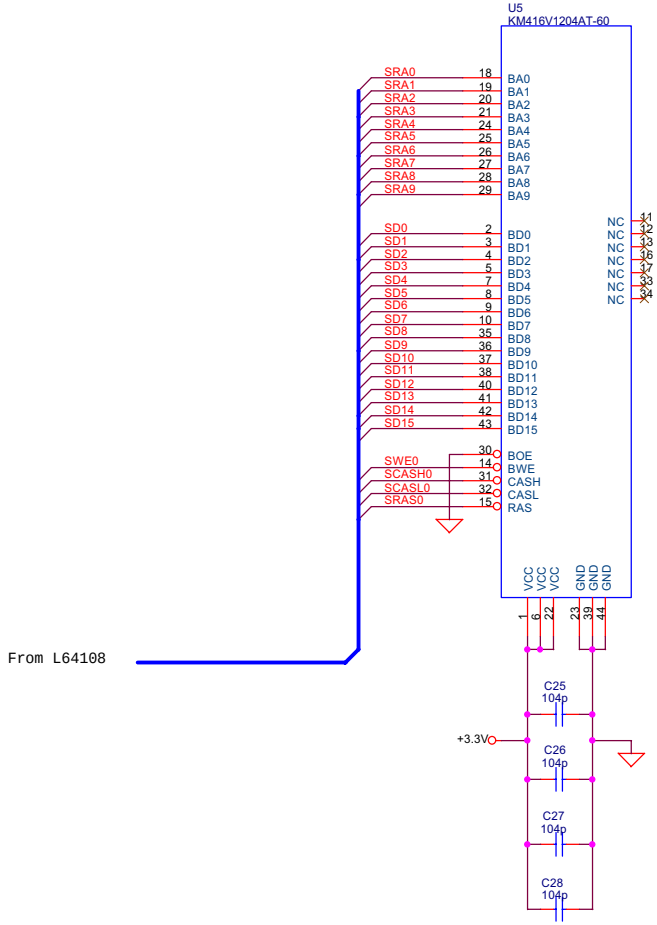
TS 2 interface



Note : This part are used in F1-SS & VA-SS model, namely without Common Interface

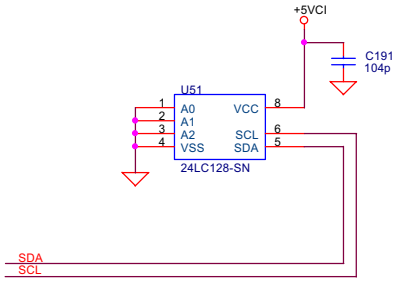
CI-OPTION			
Size: Custom	Document Number: SuperSet : CI Option		Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 9 of 36		


L64108-C
Smart Card 0
Smart Card 1
MODEM
JP1 53014-0410-OPEN
SIZE:2012
KINSEKI VCXO
*KINSEKI Option
54MHz-TEST-POINT
SOT-23
KST4401
KST4403
KDS226
KDS193
008
Document Number
SuperSet : Main CPU & Demux
Custom
Rev 1.5
Date: Wednesday, February 09, 2000
Sheet 10 of 36



RAM2M			
Size Custom	Document Number SuperSet : System memory		Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 11 of 36		

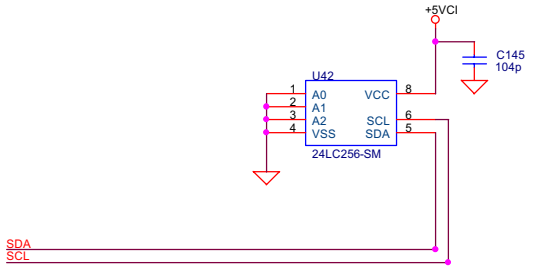
xde}



EEPROM128			
Size Custom	Document Number SuperSet :EEPROM128		Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 12 of 36		

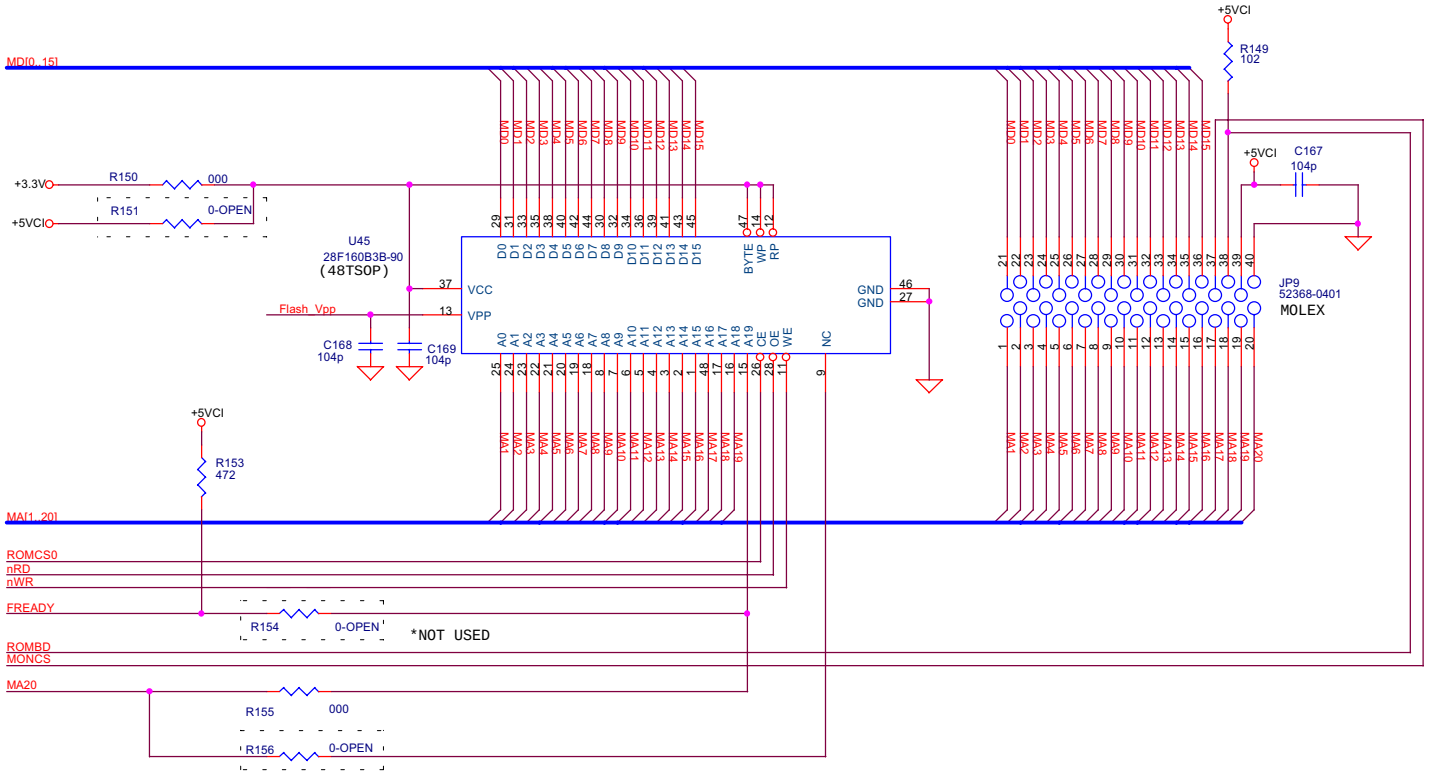
xde}

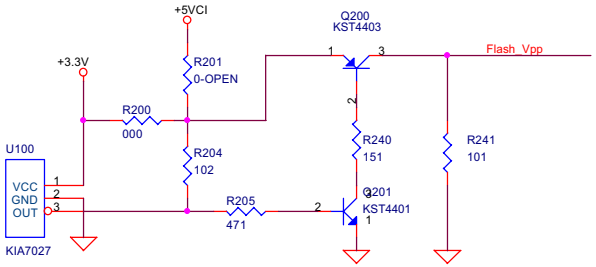
U42 & U51의 Address는 동일



Used model
: Only IQG-SS 적용

EEPROM256		
Size: Custom	Document Number: SuperSet :EEPROM256	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 13 of 36	





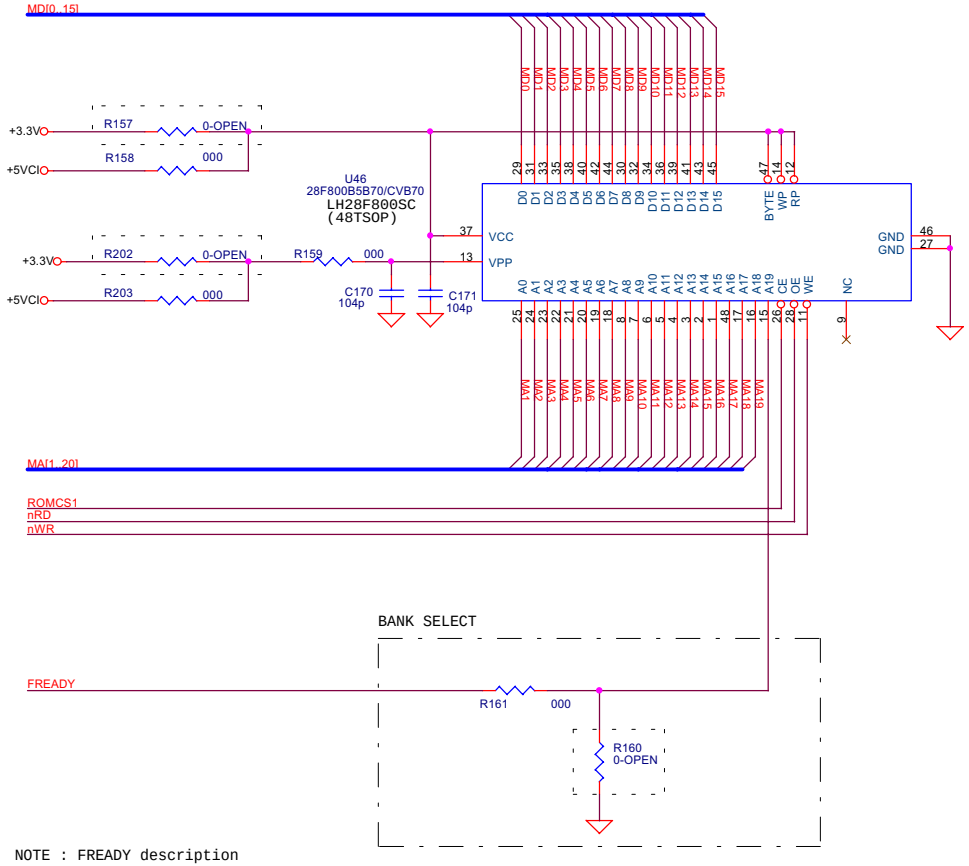
ECO A90510 : R200, 201, 152 is removed by adding extra reset for improve E-AC of Flash

Main Flash Memory is +3.3V component,open R201 and short R200

Used model

: VA-SS, VACI-SS, IQG-SS 적용

FLASH-2M		
Size: Custom	Document Number: SuperSet : Main Flash-2M	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 14 of 36	



ECO : Flash 변경에 따른 회로 변경
(28F800B5B to 28F800B3B)

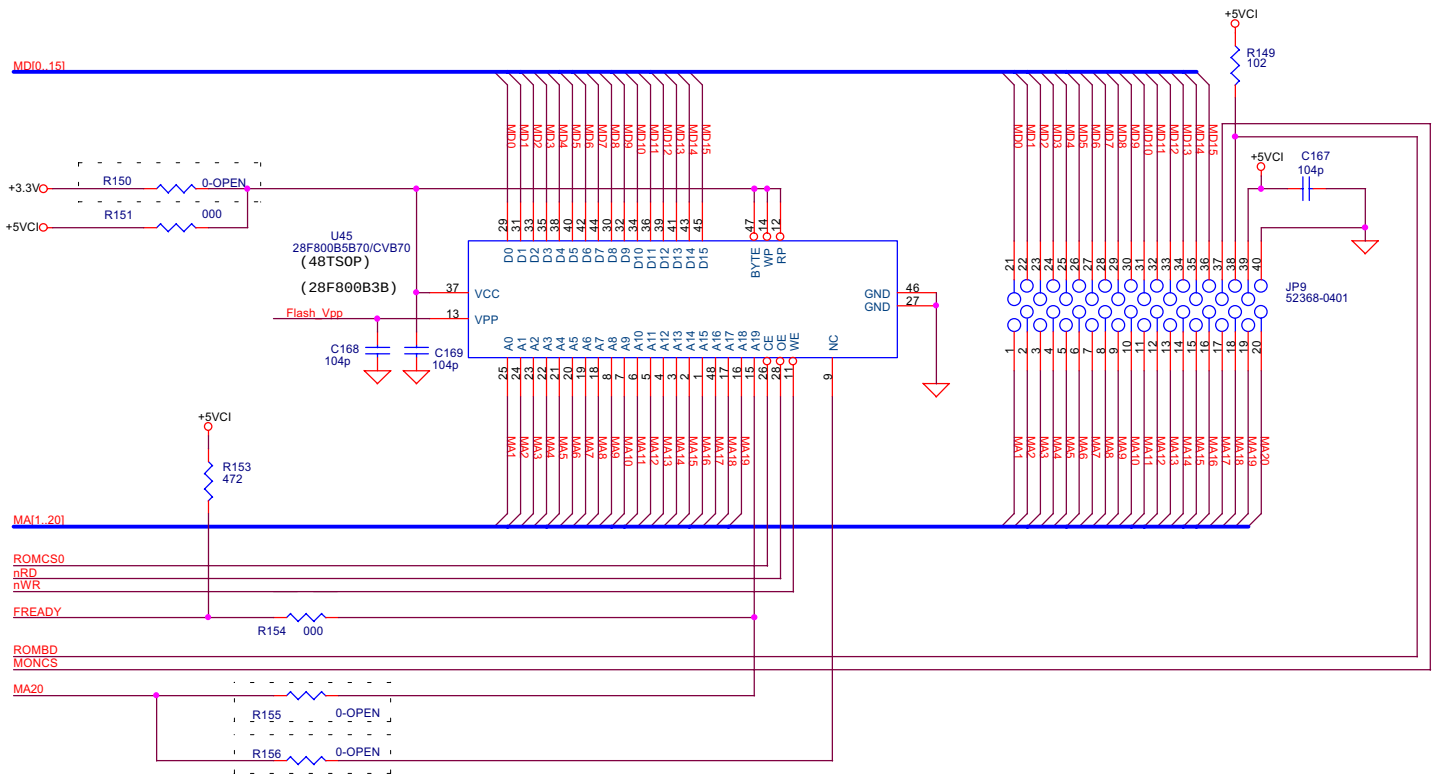
1. 삭제 : R158, 203
2. 추가 : R157, 202

NOTE : FREADY description

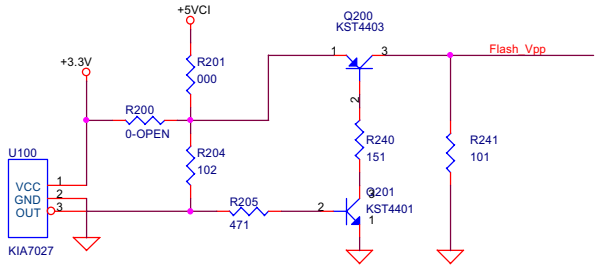
1. Main Flash 1M = FREADY not use
2. Extended Flash 1M = FREADY -> Banksel

Used model
: IQG-SS only

FLASH1M1		
Size: Custom	Document Number: SuperSet : Extended Flash memory	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 15 of 36	



* For Mitsubishi BGO Flash memory



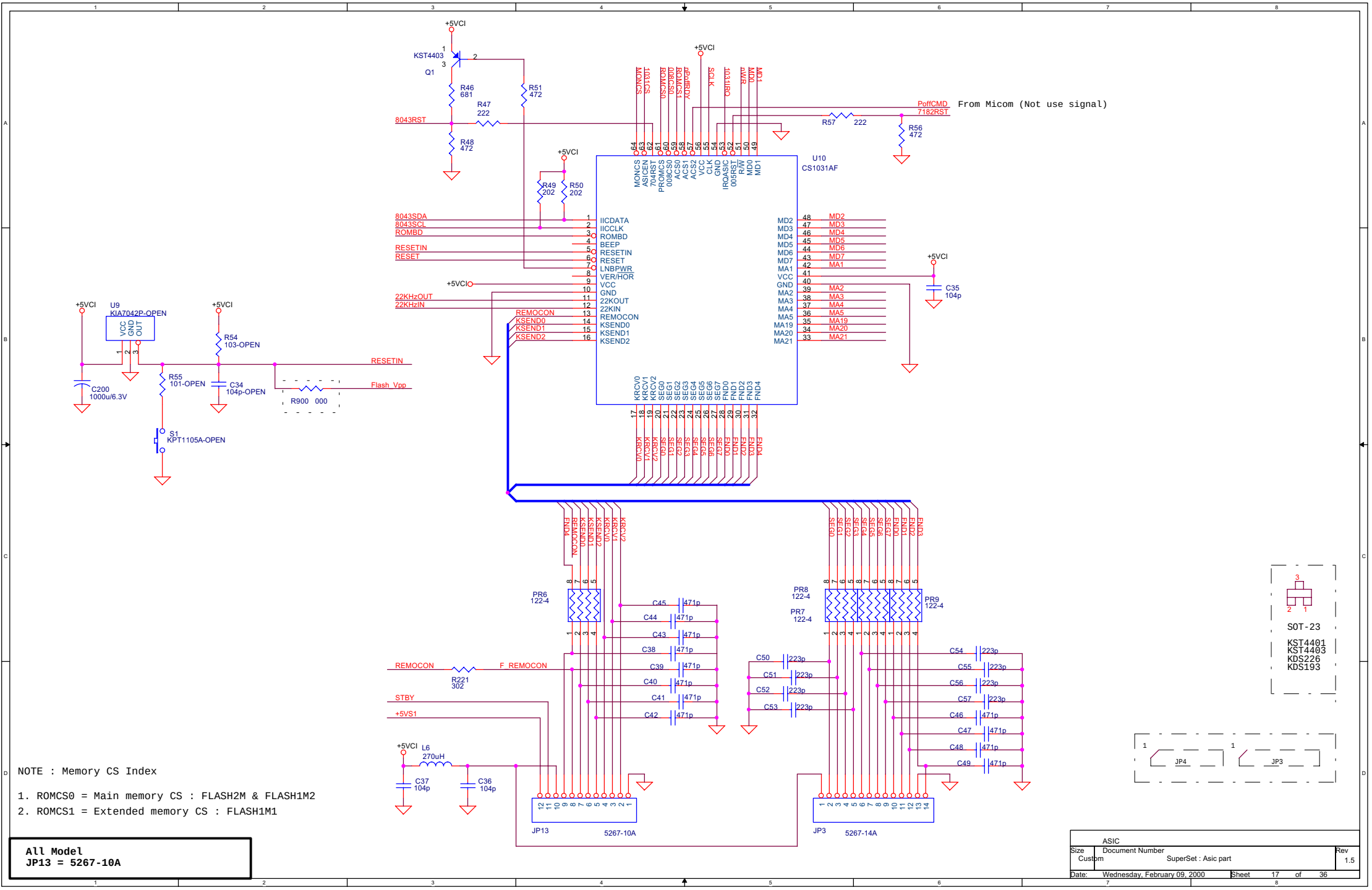
ECO A90510 : R200, 201, 152 is removed by adding extra reset for improve E-AC of Flash

1. 28F800B3B : R201 = Open, R200 = 0 ohm
2. 28F800B5B : R201 = 0 ohm, R200 = Open

Used model

: F1-SS, CI-SS 적용

FLASH1M2		
Size: Custom	Document Number: SuperSet : Main Flash-1M	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 16 of 36	

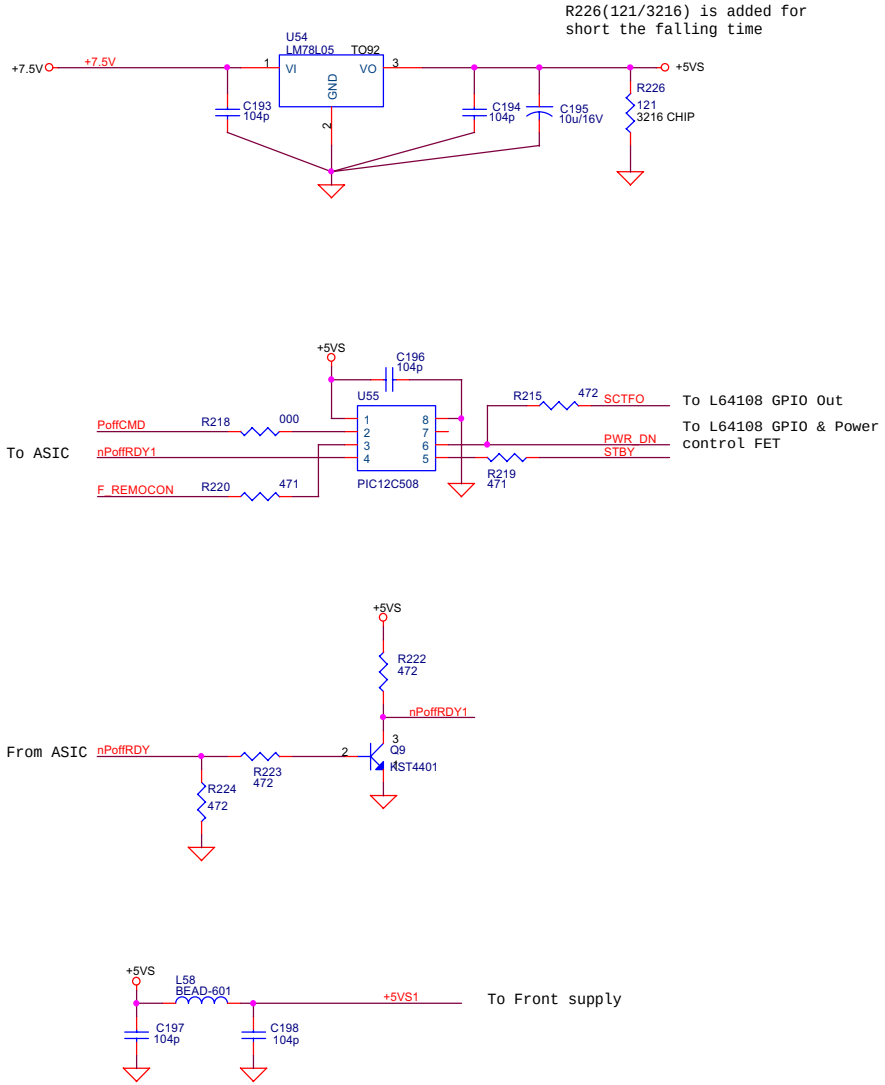


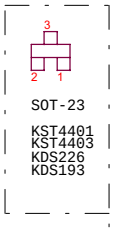
NOTE : Memory CS Index

1. ROMCS0 = Main memory CS : FLASH2M & FLASH1M2
2. ROMCS1 = Extended memory CS : FLASH1M1

All Model
JP13 = 5267-10A

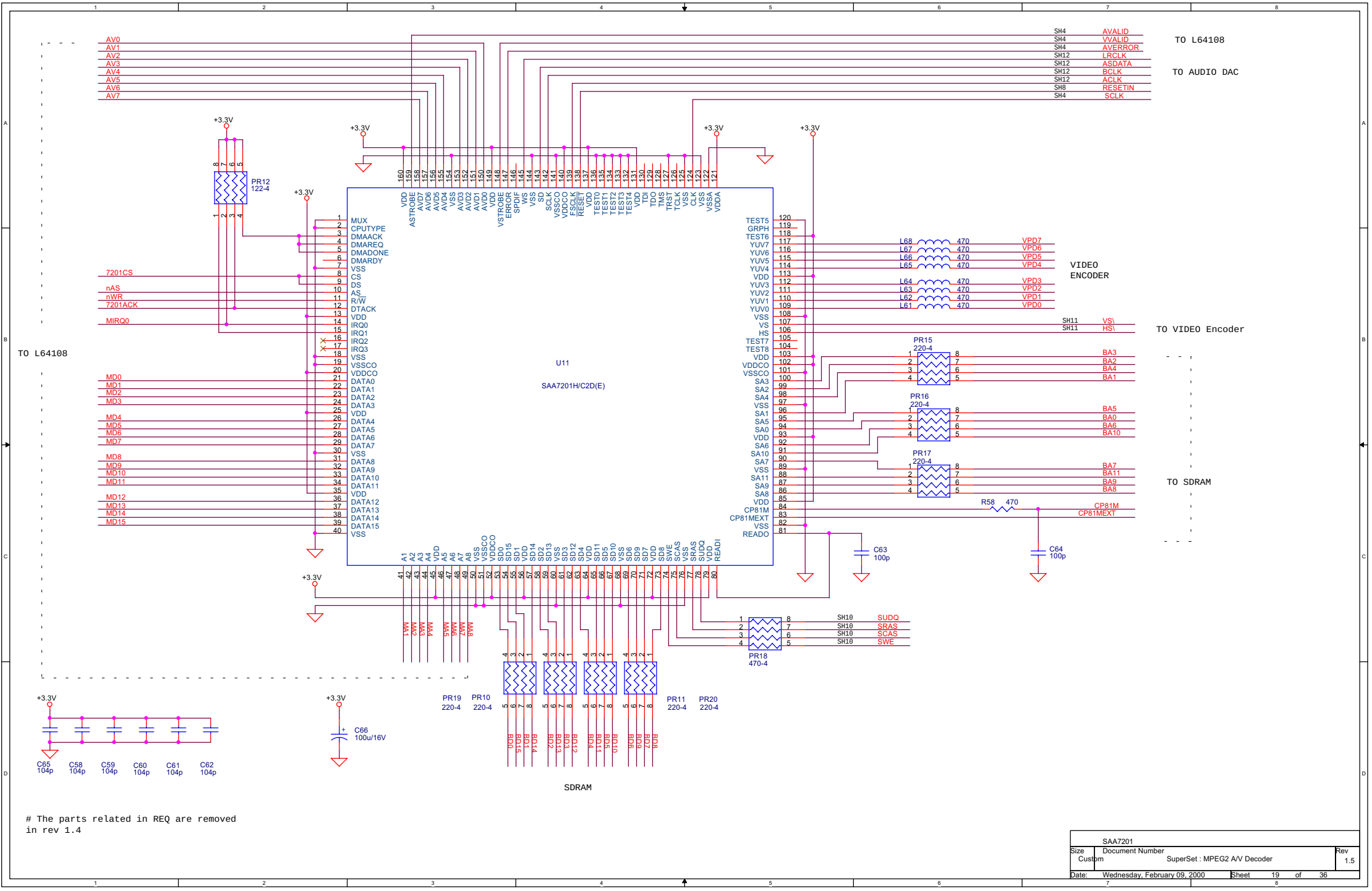
ASIC			
Size: Custom	Document Number: SuperSet : Asic part		Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 17 of 36		

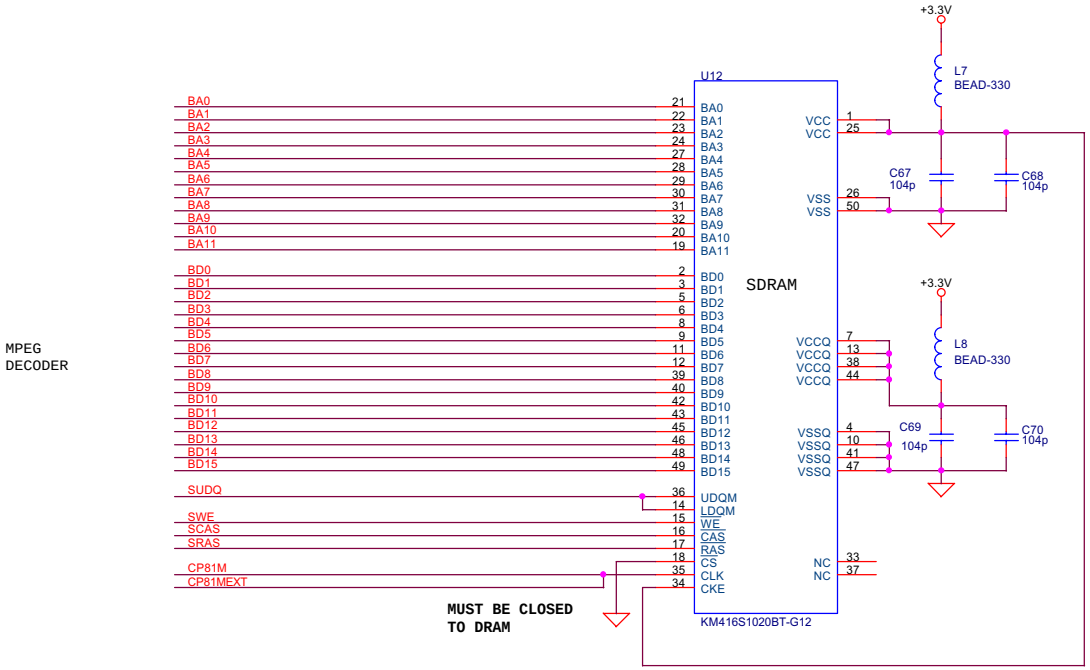




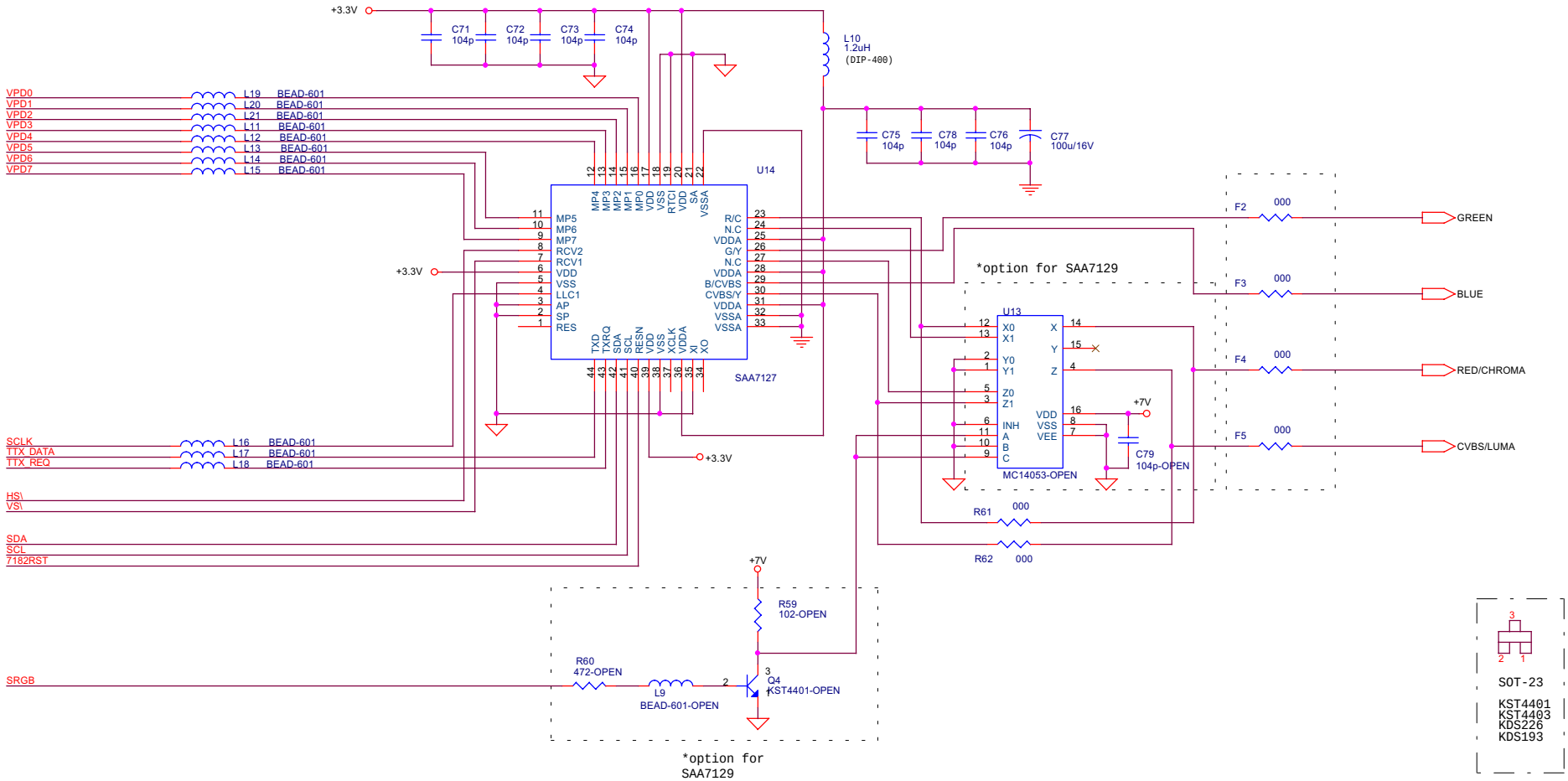
Note : MICOM is not used in all model

	MICOM		
Size Custom	Document Number SuperSet : MICOM part		Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 18 of 36		

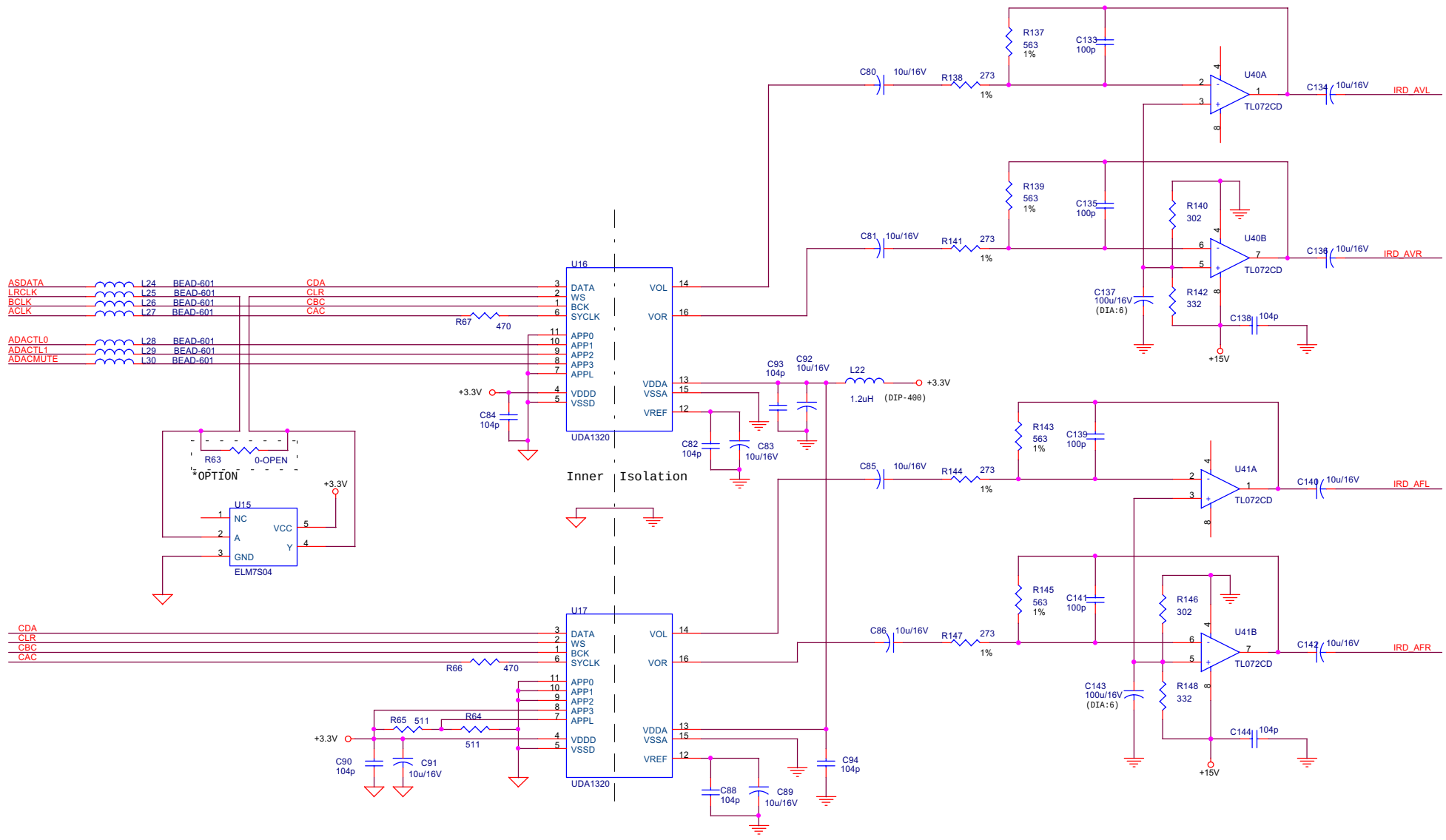

TO L64108
TO AUDIO DAC
VIDEO ENCODER
TO VIDEO Encoder
TO SDRAM
TO L64108
U11
SAA7201H/C2D(E)
SDRAM
AV0
AV1
AV2
AV3
AV4
AV5
AV6
AV7
AVALID
VVALID
AVERROR
LRCLK
ASDATA
BCLK
ACLK
RESETIN
SCLK
7201CS
nAS
nWR
7201ACK
MIRQ0
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15
VS\
HS\
BA3
BA2
BA4
BA1
BA5
BA0
BA6
BA10
BA7
BA11
BA9
BA8
CP81M
CP81MEXT
SUDQ
SRAS
SCAS
SWE
+3.3V
PR12 122-4
PR15 220-4
PR16 220-4
PR17 220-4
PR18 470-4
PR19 220-4
PR10 220-4
PR11 220-4
PR20 220-4
R58 470
C63 100p
C64 100p
C65 104p
C58 104p
C59 104p
C60 104p
C61 104p
C62 104p
C66 100u/16V
The parts related in REQ are removed in rev 1.4
SAA7201
Size Custom
Document Number
SuperSet : MPEG2 A/V Decoder
Rev 1.5
Date: Wednesday, February 09, 2000
Sheet 19 of 36



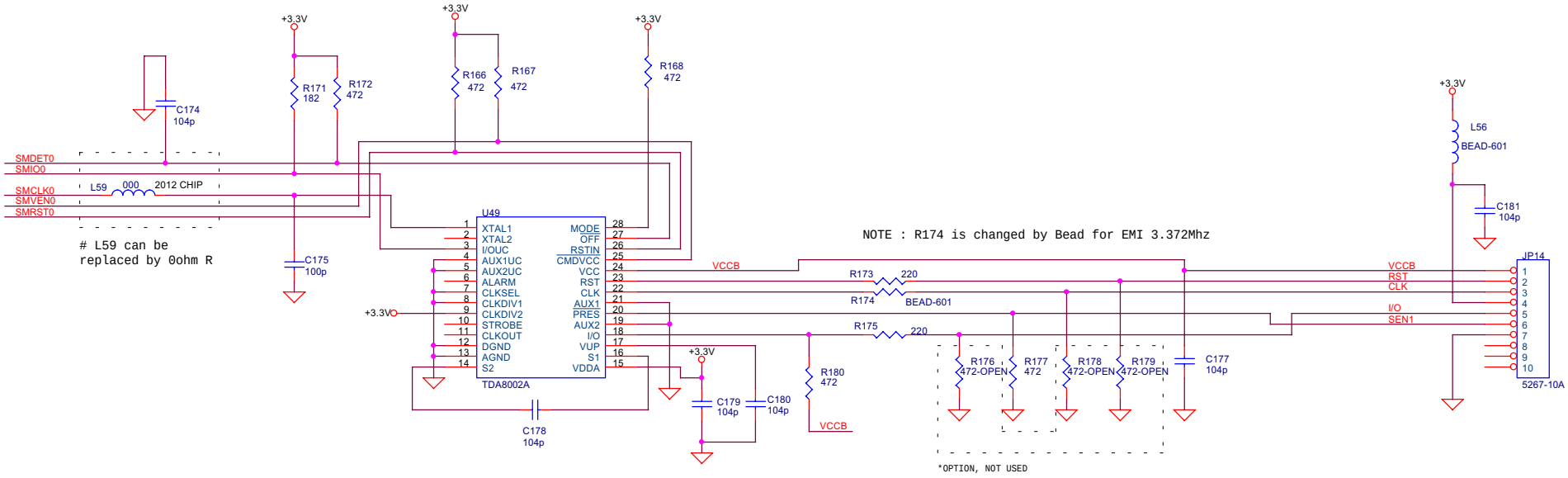
S7201MEM		
Size: Custom	Document Number: SuperSet : MPEG Decoder's buffer	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 20 of 36	



VIDEO			
Size Custom	Document Number SuperSet : Video encoder		Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 21 of 36		



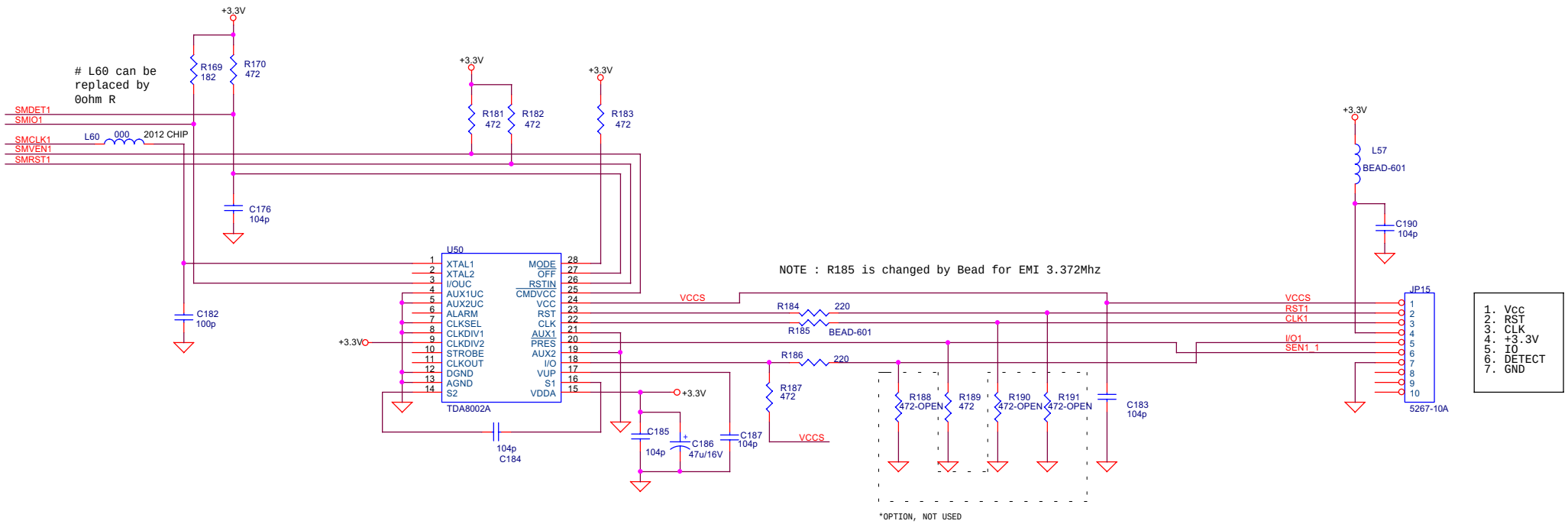
AUDIO		
Size Custom	Document Number SuperSet : Audio Part & Amp	Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 22 of 36	



Used model

: VA-SS Only (Extended Smart Card)

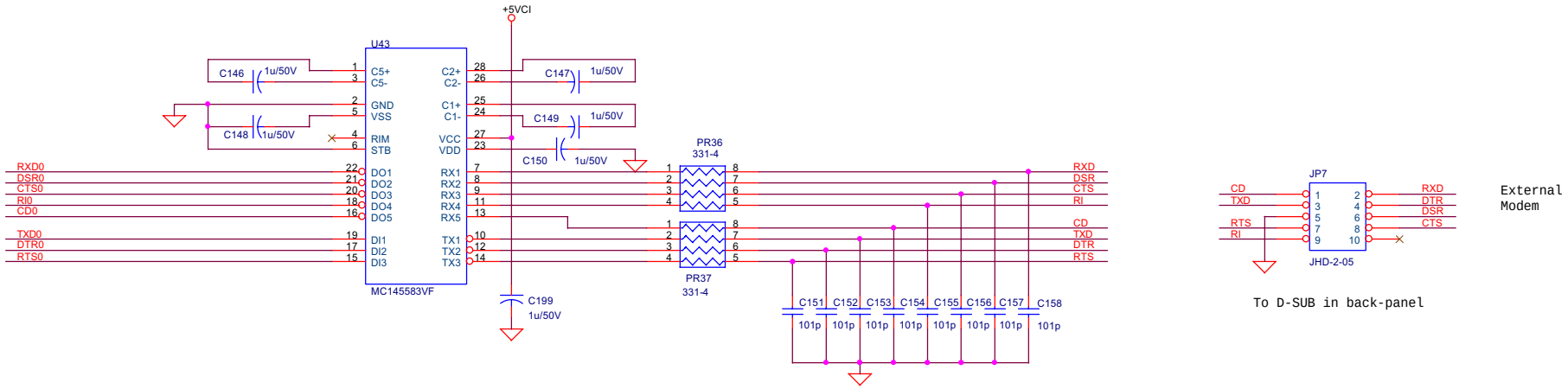
	LCARD0		
Size Custom	Document Number SuperSet : SMART CARD INTERFACE 0		Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 23 of 36		



Used model

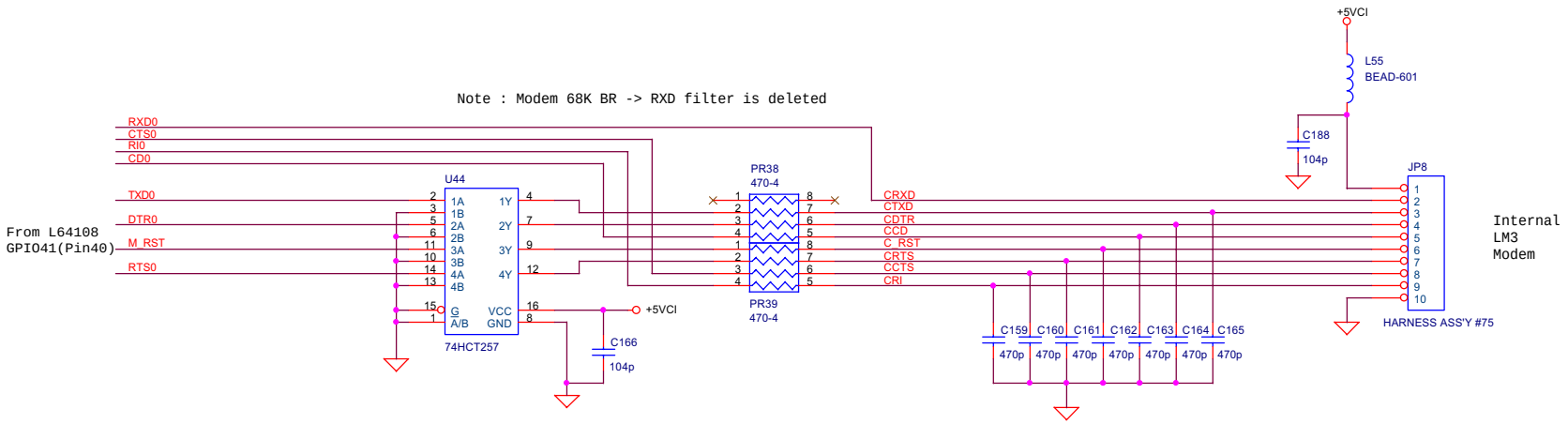
: VA-SS, VACI-SS (Main Smart Card)

LCARD 1		
Size: Custom	Document Number: SuperSet : SMART CARD INTERFACE 1	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 24 of 36	



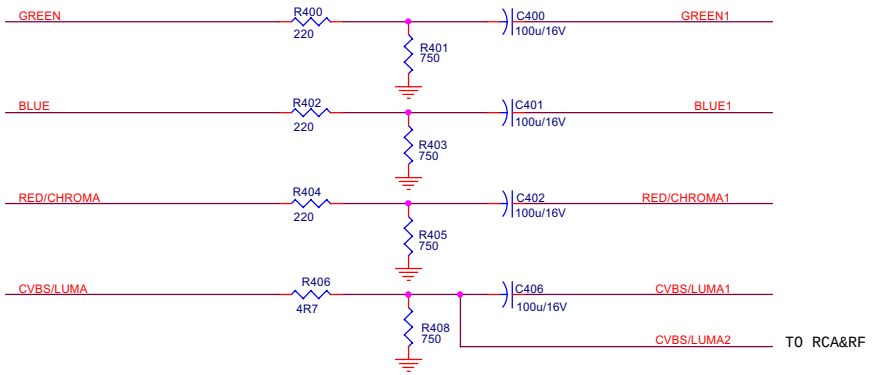
Modem은 모델 없으므로 전 부분 미삽처리

EXTMODEM			
Size Custom	Document Number SuperSet : External Modem Interface		Rev 1.5
Date: Wednesday, February 09, 2000		Sheet 25 of 36	

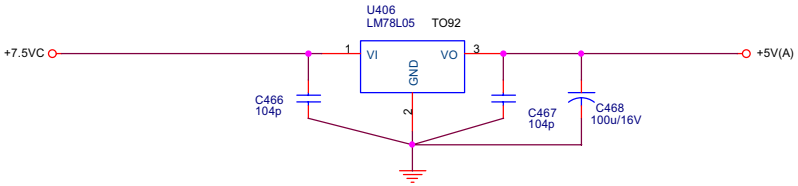


Modem은 모뎀 없으므로 전 부분 미삽처리

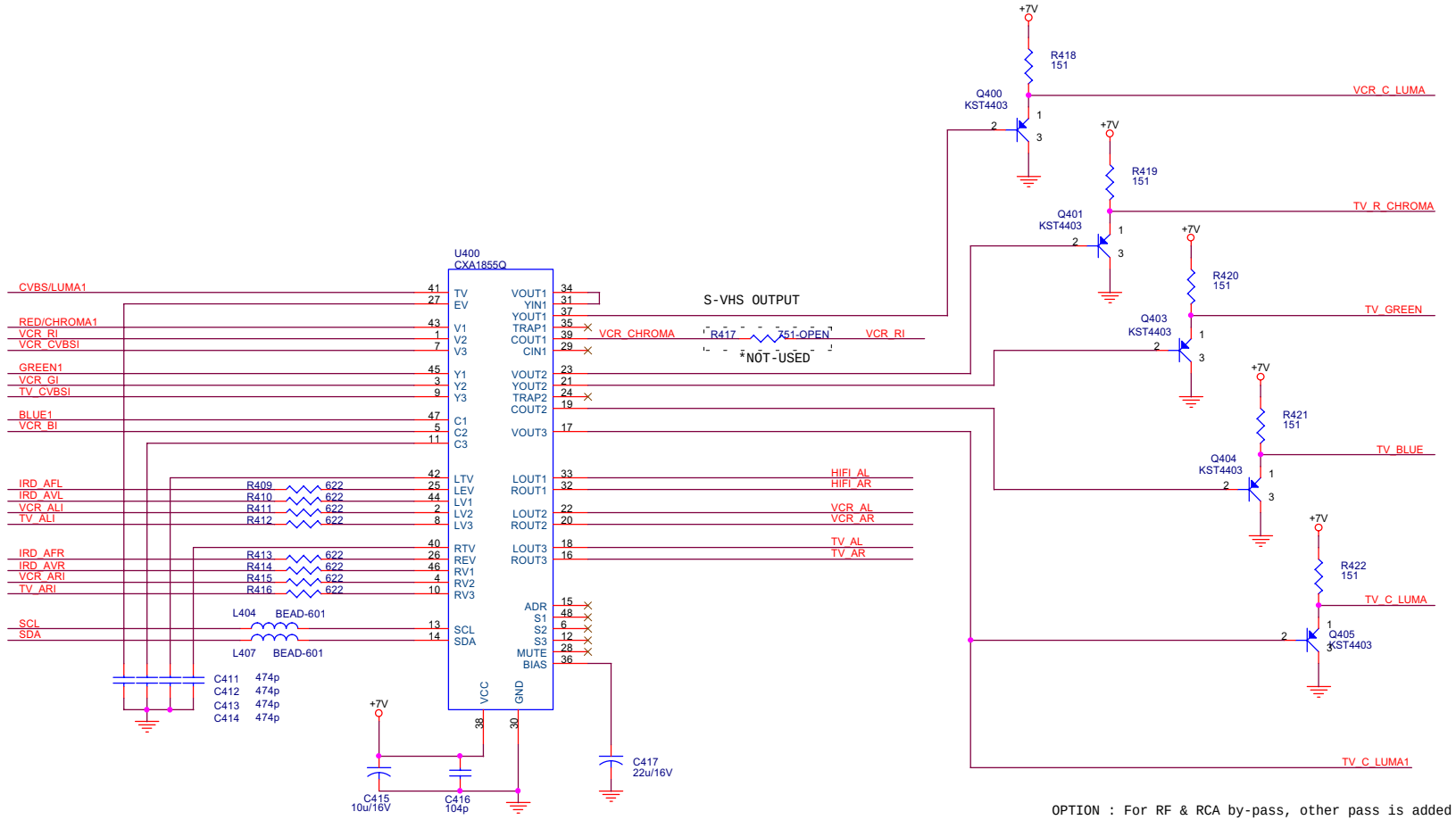
INTMODEM		
Size: Custom	Document Number: SuperSet : Internal Modem Interface	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 26 of 36	



AVCONNECT		
Size: Custom	Document Number: SuperSet : Connector Main to A/V	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 27 of 36	



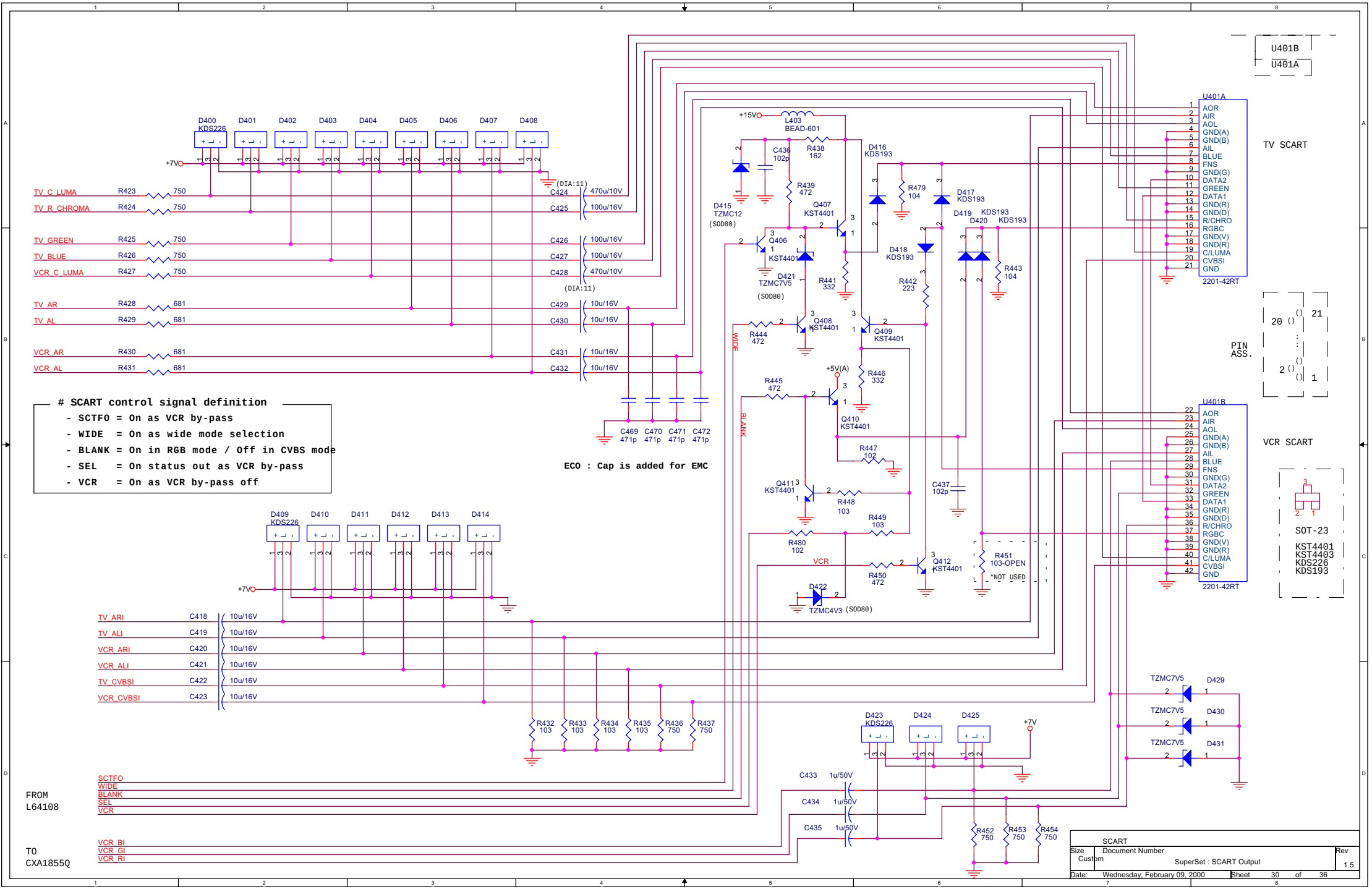
	AVPOWER		
Size Custom	Document Number	SuperSet : Linear Power(in AV B'd)	Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 28 of 36		

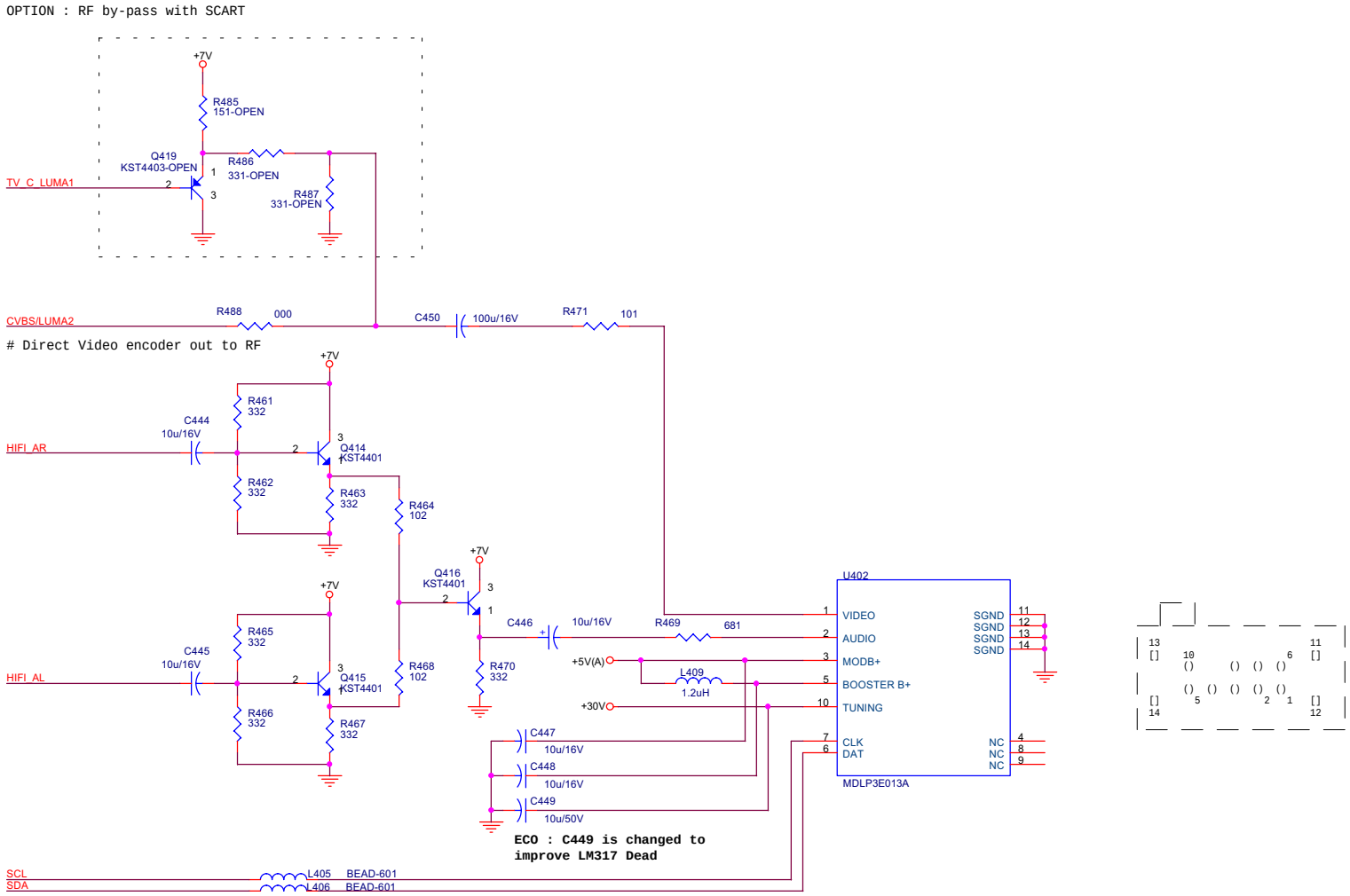


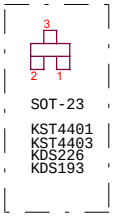
OPTION : For RF & RCA by-pass, other pass is added

Note 1 : R409, 410, 413, 414 is revalued from 0 to 622

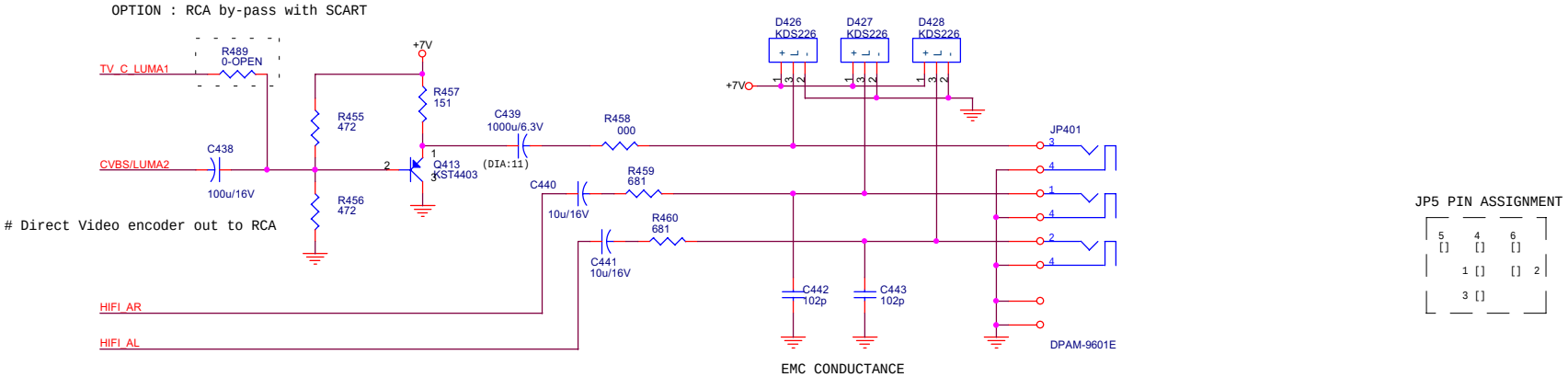
AVAMP		
Size Custom	Document Number SuperSet : A/V Amp	Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 29 of 36	


U401B
U401A
TV SCART
VCR SCART
PIN ASS.
SOT-23
KST4401
KST4403
KDS226
KDS193
2201-42RT
+7V
+15V
+5V(A)
TV_C_LUMA
TV_R_CHROMA
TV_GREEN
TV_BLUE
VCR_C_LUMA
TV_AR
TV_AL
VCR_AR
VCR_AL
TV_ARI
TV_ALI
VCR_ARI
VCR_ALI
TV_CVBSI
VCR_CVBSI
SCTFO
WIDE
BLANK
SEL
VCR
FROM L64108
TO CXA1855Q
VCR_BI
VCR_GI
VCR_RI
ECO : Cap is added for EMC
SCART control signal definition
- SCTFO = On as VCR by-pass
- WIDE = On as wide mode selection
- BLANK = On in RGB mode / Off in CVBS mode
- SEL = On status out as VCR by-pass
- VCR = On as VCR by-pass off
*NOT USED
SCART
Size Custom
Document Number
SuperSet : SCART Output
Rev 1.5
Date: Wednesday, February 09, 2000
Sheet 30 of 36





RF		
Size: Custom	Document Number: SuperSet : RF Modulator	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 31 of 36	

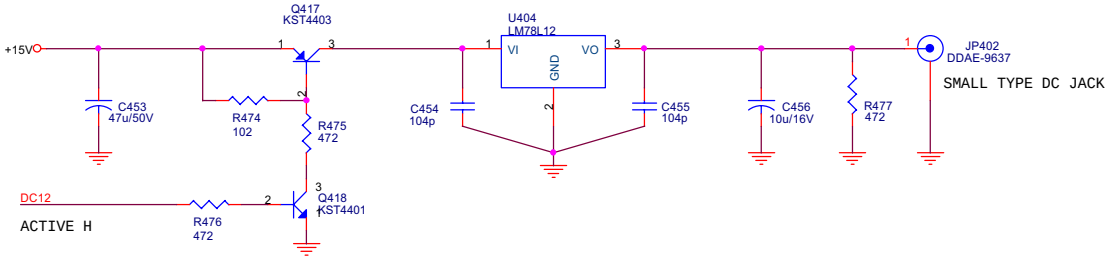


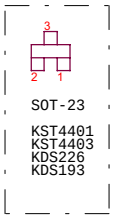
JP5 PIN ASSIGNMENT

SOT-23

KST4401
KST4403
KDS226
KDS193

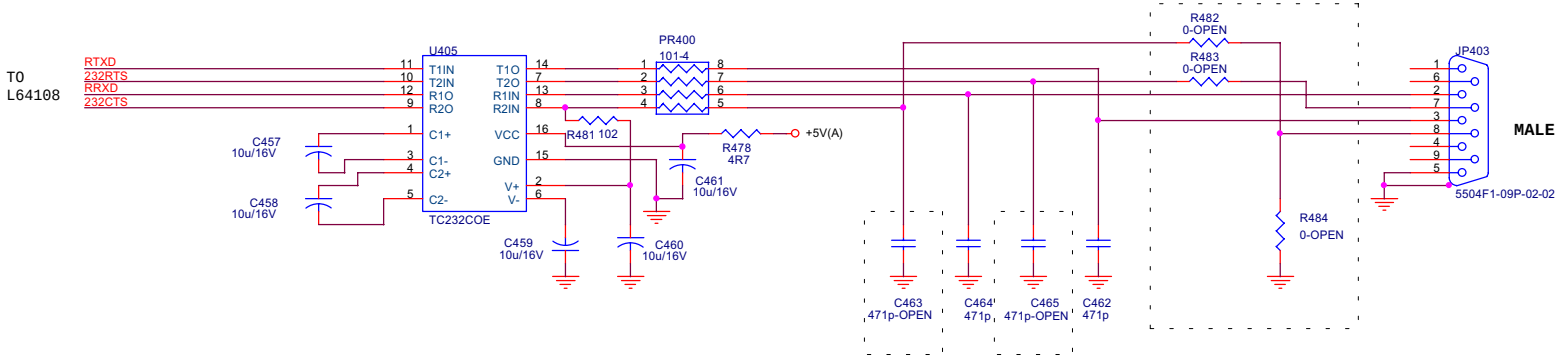
HIFI		
Size: Custom	Document Number: SuperSet : RCA Output	Rev: 1.5
Date: Wednesday, February 09, 2000	Sheet 32 of 36	



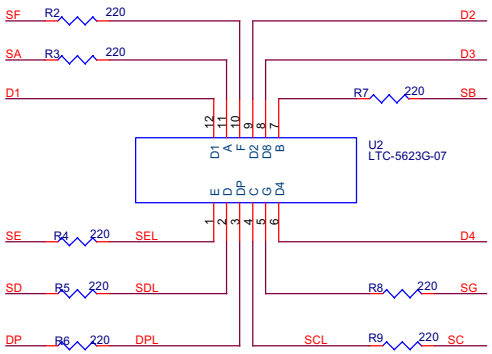


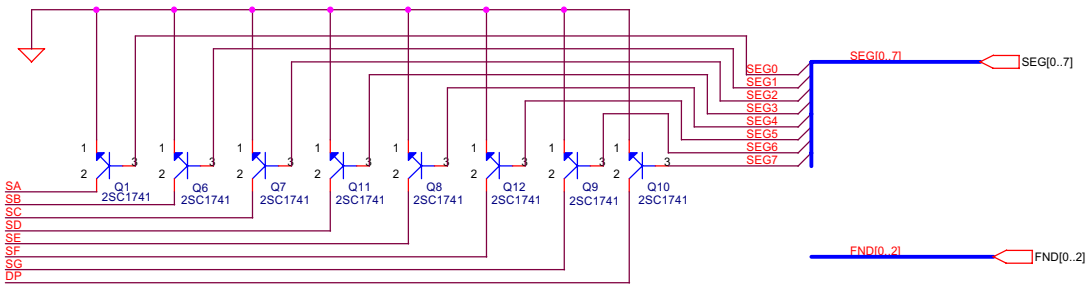
DC		
Size Custom	Document Number SuperSet : LNB Switch	Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 33 of 36	

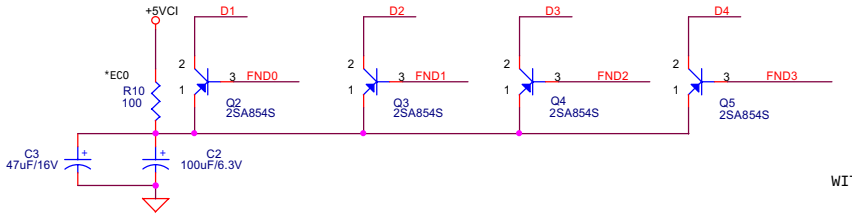
[9-Pin Serial port connector specification : Male-PC)			
Pin#	Name	Abs.	Direction
1	Data carrier detect	DCD	In
2	Receive data	Rx	In
3	Trasnmit data	Tx	Out
4	Data ternimal ready	DCD	Out
5	Signal ground	GND	
6	Data set ready	DSR	In
7	Request to send	RTS	OUT
8	Clear to send	CTS	In
9	Ring indicator	RI	In

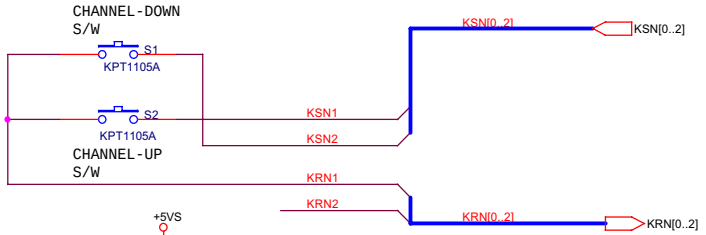


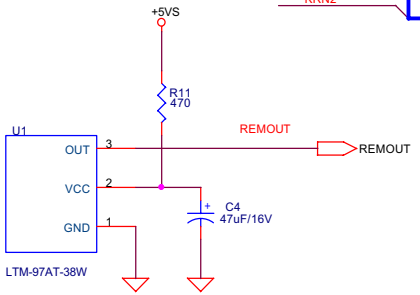
RS232			
Size Custom	Document Number SuperSet : 232C Communication		Rev 1.5
Date: Wednesday, February 09, 2000	Sheet 34 of 36		

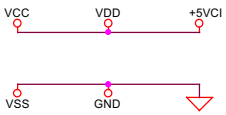


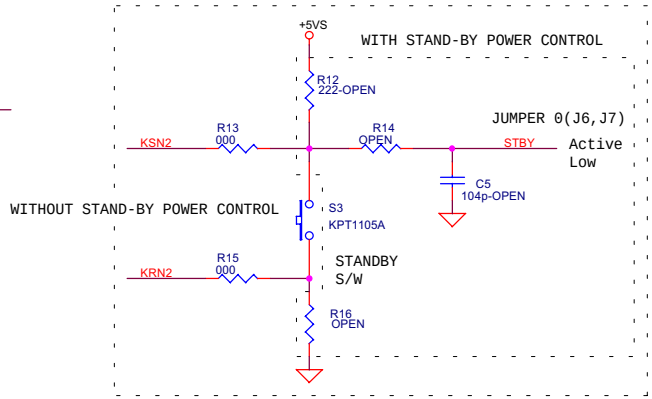


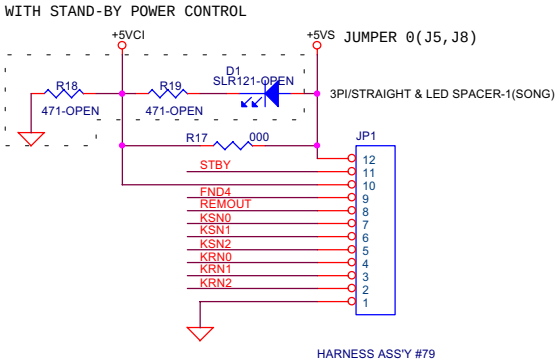


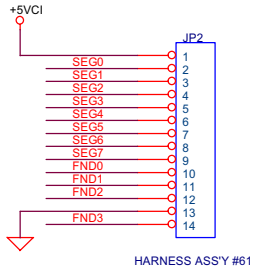










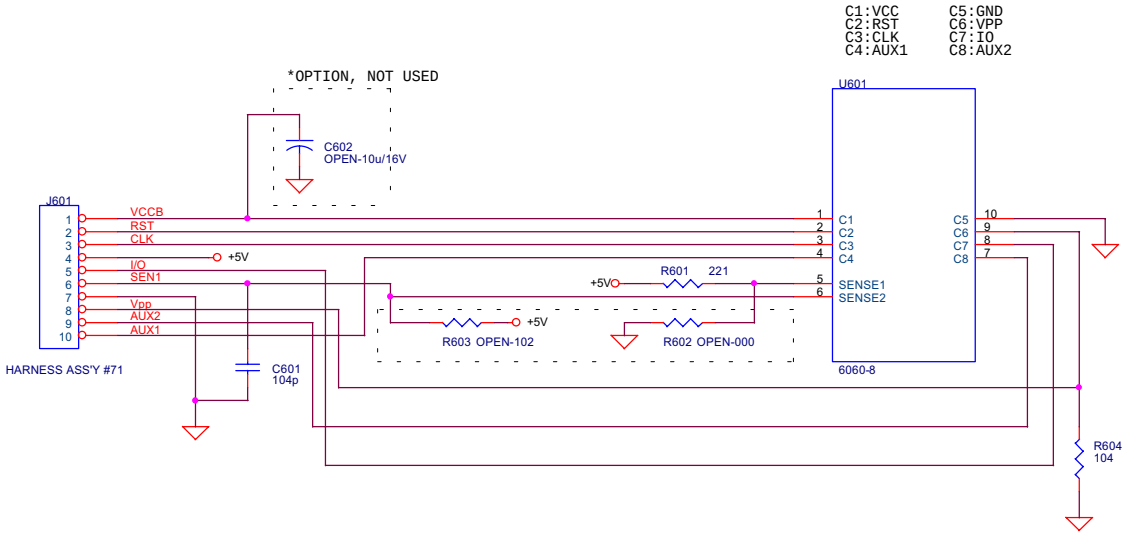


Note :

1. Extra stand-by key is added
2. Asic array stand-by key is replaced by external key
3. JP1 is changed from 10 pin to 12 pin as +5VS is added

WITH STAND-BY POWER CONTROL(USED MICOM) : JUMPER0(J1-8),D1,R12,R14,R16,R18,R19,C5
WITHOUT STAND-BY POWER CONTROL(NOT USED MICOM) : JUMPER 0(J1-4,5,8),R13,R15

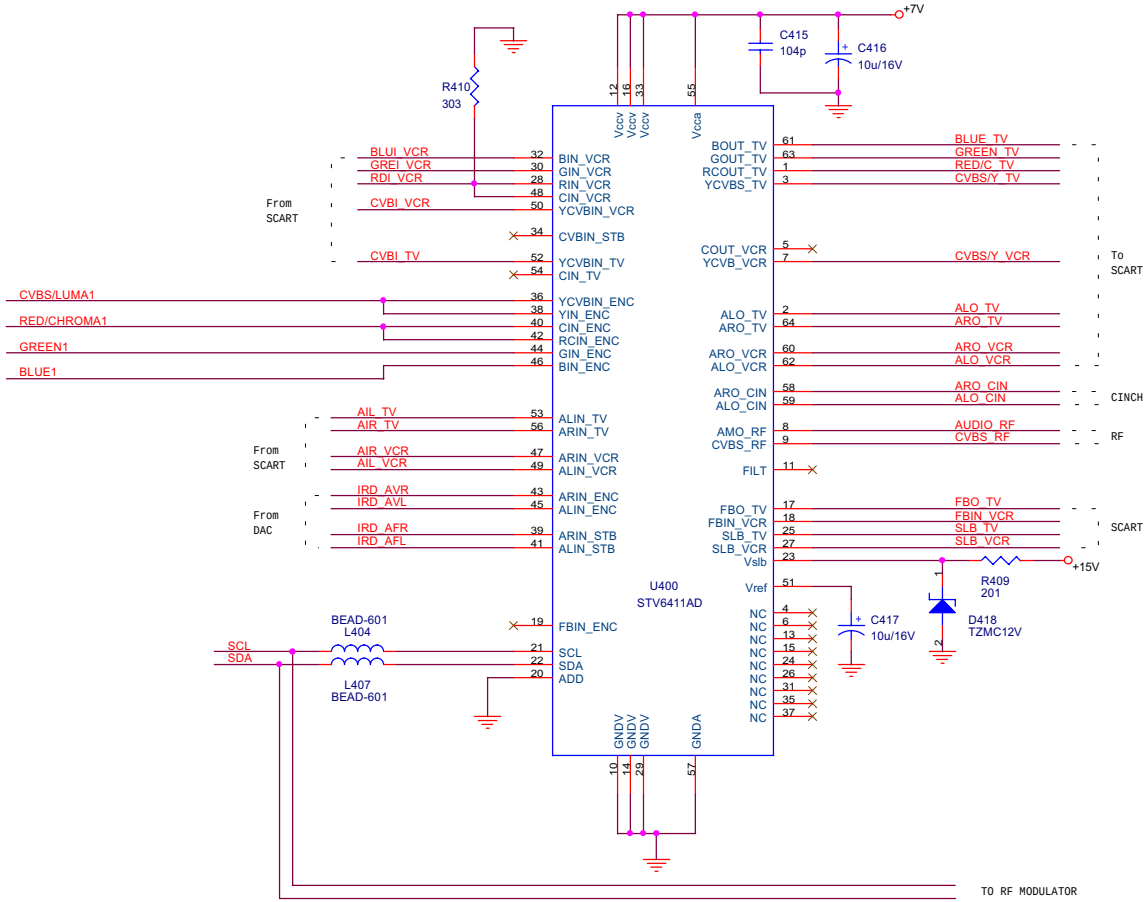
FRONT			
Size: Custom	Document Number: SuperSet : Front PCB		Rev: 1.2
Date: Wednesday, February 09, 2000	Sheet 35 of 36		



Used model

: VA-SS, VACI-SS 적용

SLOT		
Size: Custom	Document Number: SuperSet : Smart card PCB	Rev: 1.3
Date: Wednesday, February 09, 2000	Sheet 36 of 36	



NOTE : This page is only for STV 6411 version (board revision 2.0 or 2.1)

AVAMP		
Size Custom	Document Number SuperSet : A/V Amp	Rev 2.1
Date: Wednesday, February 09, 2000	Sheet 29 of 35	

BOM List(I)

MODEL CODE 15-002 F1-VACI(SUPERSET)

CODE	NAME	Q'TY	UNIT	LOCATION
15-002	**F1-VACI(SUPERSET)**			
000-0060	F-ASSY SET F1-VACI(SUPERSET)	1.0 /1	PCS	
10701-03-013	BOX CARTON HUMAX BRAND, IQG.1	1.0 /5	PCS	
000-0060	**F-ASSY SET F1-VACI(SUPERSET)**			
030-0031	ASSY ACCESSARY F1-VACI	1.0 /1	PCS	
040-0060	ASSY SET F1-VACI(SUPERSET)	1.0 /1	PCS	
10501-0660	LABEL BAR-CODE (50X15, RIBBON)	1.0 /1	PCS	
10501-0782	F1-VACI STICKER (For BOX GIFT BRAND NAME,LOGO)	1.0 /1	PCS	
10601-06-001	CUSHION PAD-PE F1,F1-CI,F1-VA,F1-VACI,IQG.1	2.0 /1	PCS	
10701-01-029	BOX GIFT (S/S, OAK)	1.0 /1	PCS	
10711-01-003	BAG VINYL "A"	1.0 /1	PCS	
10731-01-001	SILICAGEL 3g	1.0 /1	PCS	
030-0031	**ASSY ACCESSARY F1-VACI**			
01300-0004	FLY LEAD (RF CABLE)	1.0 /1	PCS	
01300-0005	CABLE POWER CORD SET	1.0 /1	PCS	
01400-0017	REMOCON / HUMAX BRAND	1.0 /1	PCS	
09900-0003	BATTERY 1.5V, "AAA"	2.0 /1	PCS	
10711-01-002	BAG VINYL "B"	1.0 /1	PCS	
10801-0312	MANUAL F1-VACI (VER HF1VACI.300)	1.0 /1	PCS	
040-0060	**ASSY SET F1-VACI(SUPERSET)**			
010-0070	ASSY SC B/D F1-VACI,F1-VA	1.0 /1	PCS	
010-0082	ASSY CPU B/D F1-VACI(SUPERSET)	1.0 /1	PCS	
010-0092	ASSY FEC B/D (SUPERSET:TDA 8044 적용 B/D)	1.0 /1	PCS	
01403-0012	POWER SMPS / SY-T2801 (REV 3.0)	1.0 /1	PCS	
020-0088	ASSY FRONT F1-VACI	1.0 /1	PCS	
050-0071	ASSY BOTTOM F1,F1-CI,F1-VA,F1-VACI(SUPERSET)	1.0 /1	PCS	
060-0004	ASS'Y POWER S/W(WITH HARNESS #82)	1.0 /1	PCS	
10011-04-006	PANEL BACK F-SERIES	1.0 /1	PCS	
10021-03-003	CASE TOP F-SERIES,IQG.1	1.0 /1	PCS	
10081-10-001	PAPER WASHER (PAI 7.8X0.8T;내측 PAI 3.3T)	1.0 /1	PCS	
10101-08-001	SMART NUT	2.0 /1	PCS	ASSY FRONT+ASSY SC B/D(2EA)
10501-0660	LABEL BAR-CODE (50X15, RIBBON)	1.0 /1	PCS	
1100300804	SCREW T/T 2S P/H BLK (03*8)	1.0 /1	PCS	ASSY CPU B/D(RCA)+PANEL BACK(1EA)
1105300804	SCREW T/T 2S B/H BLK (03*8)	4.0 /1	PCS	ASSY CPU B/D(SCART)+PANEL BACK(2EA),ASSY PS B/D+PANEL BACK(2EA)
1115300504	SCREW T/T 3S B/H BLK (03*5)	9.0 /1	PCS	ASSY FRONT+CASE BOTTOM(2EA),CASE TOP+CASE BOTTOM(3EA),PANEL BACK+CASE BOTTOM(3EA), ASSY CPU B/D(RF MODULATOR)+PANEL BACK(1EA)
1115300602	SCREW T/T 3S B/H NAT (03*6)	14.0 /1	PCS	ASSY CPU B/D+CASE BOTTOM(7EA),POWER SMPS+CASE BOTTOM(4EA),ASSY FEC B/D+CASE BOTTOM(3EA)

BOM List(I)

MODEL CODE 15-002 F1-VACI(SUPERSET)

CODE	NAME	Q'TY	UNIT	LOCATION
1115400504	SCREW T/T 3S B/H BLK (04*5)	4.0 /1	PCS	CASE TOP+CASE BOTTOM(4EA)
1118300602	SCREW T/T 3S PHW NAT(03*6)	2.0 /1	PCS	ASSY FRONT+ASSY SC B/D(2EA)
1211210002	NUT UNF 3/8INCH*32	2.0 /1	PCS	ASSY FEC B/D(TUNER)+PANEL BACK(2EA)
1231111002	WASHER PAI10	2.0 /1	PCS	ASSY FEC B/D(TUNER)+PANEL BACK(2EA)
010-0070	ASSY SC B/D F1-VACI,F1-VA			
00104-0001	CAP MULTI CERAMIC-A 0.1uF/104/+80~-20%	1.0 /1	PCS	C601
00203-0004	RES CARBON 100K,1/4W,5%	1.0 /1	PCS	R604
00203-0018	RES CARBON 220,1/4W,5%	1.0 /1	PCS	R601
00999-0016	CON SMART CONNECTOR 6060-08-2	1.0 /1	PCS	U601
01004-0075	PCB SC B/D (SUPERSET) REV 1.3	1.0 /1	PCS	
01301-0062	HARNESS ASSY#71 (10PIN)	1.0 /1	PCS	J601
010-0082	ASSY CPU B/D F1-VACI(SUPERSET)			
00003-0006	IC ASIC CS1031AF/64pin/QFP	1.0 /1	PCS	U10
00004-0006	IC D-RAM KM416V1204AT-60	1.0 /1	PCS	U5
00004-0007	IC SD-RAM K4S161622D/TSOP II	1.0 /1	PCS	U12
00006-0007	IC OP AMP TL072CD/SOP	2.0 /1	PCS	U40,41
00007-0008	IC EEPROM 24LC128SN	1.0 /1	PCS	U51
00009-0002	IC REGULATOR 78L05/TO-92	1.0 /1	PCS	U406
00009-0008	IC REGULATOR 78L12/TO-92	1.0 /1	PCS	U404
00010-0026	IC DEMUX & CPU L64108(REV:C)	1.0 /1	PCS	U4
00010-0028	IC MPEG-2 DECODER SAA7201H(VER:C2E)	1.0 /1	PCS	U11
00011-0006	IC VIDEO ENCODER SAA7127H/QFP44	1.0 /1	PCS	U14
00012-0006	IC CMOS 74HC14/14pin/SOP	1.0 /1	PCS	U28
00012-0016	IC CMOS 74HC257/SOP	7.0 /1	PCS	U21-23,32-34,36
00012-0018	IC CMOS 74HC244/SOP	6.0 /1	PCS	U19,24,25,29-31
00012-0026	IC CMOS 74HCT244/SOP	1.0 /1	PCS	U20
00012-0027	IC CMOS 1-INPUT INVERTER ELM7S04	1.0 /1	PCS	U15
00012-0038	IC CMOS 74HC00	1.0 /1	PCS	U27
00013-0003	IC FLASH MEMORY 16MB 28F160B3B-90	1.0 /1	PCS	U45
00014-0007	IC DAC UDA1320/SSOP16	2.0 /1	PCS	U16,17
00016-0001	IC C/I CONTROLLER CXD1957AQ/QFP80	1.0 /1	PCS	U26
00017-0002	IC RS232 DRIVER ADM232LJR	1.0 /1	PCS	U405
00099-0050	IC AUDIO/VIDEO MUX CXA1855Q	1.0 /1	PCS	U400
00099-0051	IC SMART CARD TDA8002A	1.0 /1	PCS	U50
00099-0052	IC VOLTAGE DETECTOR KIA7027AF/SOT-89	1.0 /1	PCS	U100
00106-0042	CAP MULTI CERAMIC-CHIP 0.1uF/104p/25V/Y5V/1608	80.0 /1	PCS	C3,4,9-16,19,25-28,35-37,58-62,65,67-76,78,82,84,88,90,93-106,114-118,120,122-124,131,138,144, 167-169,176,183-185,187,190,191,416,454,455,466,467
00106-0048	CAP MULTI CERAMIC-CHIP 10pF/100p/25V/C0G/1608	7.0 /1	PCS	C63,64,133,135,139,141,182
00106-0052	CAP MULTI CERAMIC-CHIP 0.001uF/102p/25V/X7R/1608	6.0 /1	PCS	C107,113,436,437,442,443
00106-0054	CAP MULTI CERAMIC-CHIP 0.0047uF/472p/25V/X7R/1608	1.0 /1	PCS	C24
00106-0055	CAP MULTI CERAMIC-CHIP 0.0068uF/682p/25V/X7R/1608	2.0 /1	PCS	C108,125

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MODEL CODE 15-002 F1-VACI(SUPERSET)

CODE	NAME	Q'TY	UNIT	LOCATION
00106-0057	CAP MULTI CERAMIC-CHIP 470pF/471p/25V/C0G/1608	18.0 /1	PCS	C38-49,462,464,469-472
00106-0059	CAP MULTI CERAMIC-CHIP 0.022uF/223p/25V/X7R/1608	8.0 /1	PCS	C50-57
00106-0068	CAP MULTI CERAMIC-CHIP 22pF/220p/25V/C0G/1608	1.0 /1	PCS	C22
00106-0077	CAP MULTI CERAMIC-CHIP 0.0015uF/152p/25V/X7R/1608	1.0 /1	PCS	C21
00106-0080	CAP MULTI CERAMIC-CHIP 0.47uF/474/16V/Y5V/2012	6.0 /1	PCS	C23,201,411-414
00106-0097	CAP MULTI CERAMIC-CHIP 0.1uF/104p/50V/X7R/3216	1.0 /1	PCS	C18
00107-0000	CAP ELE 470uF/10V/SSL	2.0 /1	PCS	C424,428
00107-0001	CAP ELE 100uF/16V/SSL	16.0 /1	PCS	C1,66,77,132,137,143,400-402,406,425-427,438,450,468
00107-0003	CAP ELE 22uF/16V/SSL	1.0 /1	PCS	C417
00107-0005	CAP ELE 47uF/16V/SSL	1.0 /1	PCS	C186
00107-0017	CAP ELE 1uF/50V/SSL	7.0 /1	PCS	C110-112,126,433-435
00107-0057	CAP ELE 10uF/16V/SSL	36.0 /1	PCS	C80,81,83,85,86,89,91,92,134,136,140,142,415,418-423,429-432,440,441,444-448,456-461
00107-0066	CAP ELE 1000uF/6.3V/SSL/BULK	1.0 /1	PCS	C20
00107-0067	CAP ELE 47uF/50V/SSL	1.0 /1	PCS	C453
00107-0078	CAP ELE 1000uF/6.3V/SHL	2.0 /1	PCS	C200,439
00107-0087	CAP ELE 10uF/50V/SSL	1.0 /1	PCS	C449
00200-0000	RES CHIP 0, 5%, 2012	3.0 /1	PCS	L60,R196,197
00200-0087	RES CHIP 4.7K, 5%, 1608	57.0 /1	PCS	R10,11,18,19,25-30,34-37,48,51,56,80,81,85,87,89,90-92,95,108,109,111,112,117,119,120,153,170,181-183, 187,189,212,214,217,227-229,231,280,439,444,445,450,455,456,475-477
00200-0088	RES CHIP 470, 5%, 1608	1.0 /1	PCS	R205
00200-0089	RES CHIP 20, 5%, 1608	1.0 /1	PCS	R16
00200-0090	RES CHIP 0, 5%, 1608	11.0 /1	PCS	R9,61,62,150,155,200,206,207,458,488,900
00200-0093	RES CHIP 22K, 5%, 1608	1.0 /1	PCS	R442
00200-0094	RES CHIP 1K, 5%, 1608	13.0 /1	PCS	R17,83,116,149,204,216,282,447,464,468,474,480,481
00200-0096	RES CHIP 10K, 5%, 1608	29.0 /1	PCS	R3,8,14,15,23,77,82,84,93,94,106,110,113-115,133-136,208-211,432-435,448,449
00200-0097	RES CHIP 100K, 5%, 1608	25.0 /1	PCS	R22,68-76,78,79,96-105,107,443,479
00200-0098	RES CHIP 47, 5%, 1608	12.0 /1	PCS	R12,58,66,67,L61-68
00200-0099	RES CHIP 4.7, 5%, 1608	2.0 /1	PCS	R406,478
00200-0100	RES CHIP 100, 5%, 1608	2.0 /1	PCS	R241,471
00200-0104	RES CHIP 22, 5%, 1608	5.0 /1	PCS	R184,186,400,402,404
00200-0105	RES CHIP 3.3K, 5%, 1608	11.0 /1	PCS	R142,148,441,446,461-463,465-467,470
00200-0106	RES CHIP 75, 5%, 1608	14.0 /1	PCS	R401,403,405,408,423-427,436,437,452-454
00200-0112	RES CHIP 150, 5%, 1608	7.0 /1	PCS	R240,418-422,457
00200-0113	RES CHIP 750, 5%, 1608	1.0 /1	PCS	R13
00200-0120	RES CHIP 680, 5%, 1608	8.0 /1	PCS	R46,428-431,459,460,469
00200-0121	RES CHIP 2.7K, 5%, 1608	1.0 /1	PCS	R24(ONLY WITH KINSEKI VCXO)
00200-0122	RES CHIP 6.2K, 5%, 1608	8.0 /1	PCS	R409-416
00200-0135	RES CHIP 27K, 1%, 1608	4.0 /1	PCS	R138,141,144,147
00200-0142	RES CHIP 2.2K, 5%, 1608	4.0 /1	PCS	R4,5,47,57
00200-0146	RES CHIP 68, 5%, 1608	1.0 /1	PCS	R20
00200-0147	RES CHIP 1K, 1%, 1608	1.0 /1	PCS	R21
00200-0148	RES CHIP 2K, 5%, 1608	2.0 /1	PCS	R49,50
00200-0150	RES CHIP 1.6K, 5%, 1608	1.0 /1	PCS	R438
00200-0171	RES CHIP 120, 5%, 3216	2.0 /1	PCS	R86,118

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MODEL CODE 15-002 F1-VACI(SUPERSET)

CODE	NAME	Q'TY	UNIT	LOCATION
00200-0173	RES CHIP 0, 5%, 3216	4.0 /1	PCS	F2-5
00200-0179	RES CHIP 56K, 1%, 1608	4.0 /1	PCS	R137,139,143,145
00200-0200	RES CHIP 1.8K, 5%, 1608	1.0 /1	PCS	R169
00200-0204	RES CHIP 510, 5%, 1608	2.0 /1	PCS	R64,65
00200-0215	RES CHIP 3K, 5%, 1608	3.0 /1	PCS	R140,146,221
00207-0001	RES CHIP NETWORK 22*4	7.0 /1	PCS	PR10,11,15-17,19,20
00207-0002	RES CHIP NETWORK 100*4	1.0 /1	PCS	PR400
00207-0004	RES CHIP NETWORK 1.2K*4	5.0 /1	PCS	PR6-9,12
00207-0006	RES CHIP NETWORK 47*4	17.0 /1	PCS	PR1-4,18,21,23-25,27,28,30-35
00207-0012	RES CHIP NETWORK 4.7K*8(R-CIRCUIT)	1.0 /1	PCS	PR5
00301-0017	DIODE ZENER TZM5240B(10V)/SOD80	3.0 /1	PCS	D1-3
00301-0018	DIODE ZENER TZM5242B(12V)/SOD80	1.0 /1	PCS	D415
00301-0019	DIODE ZENER TZM5229(4.3V)/SOD80	1.0 /1	PCS	D422
00301-0020	DIODE ZENER TZM5236B(7.5V)/SOD80	4.0 /1	PCS	D421,429-431
00304-0001	DIODE SWITCHING KDS193/SOT-23	5.0 /1	PCS	D416-420
00304-0005	DIODE SWITCHING KDS226/DAN217/SOT-23	21.0 /1	PCS	D400-414,423-428
00400-0007	TR CHIP KST4401/NPN/SOT-23	15.0 /1	PCS	Q5,6,8,201,406-412,414-416,418
00400-0008	TR CHIP KST4403/PNP/SOT-23	9.0 /1	PCS	Q1,200,400,401,403-405,413,417
00402-0000	FET IRF7303/SOP	3.0 /1	PCS	U18,52,53
00502-0000	VCXO 27MHZ (DJVF-3H5T27.000MHZ)	1.0 /1	PCS	U2(ONLY WITH KINSEKI VCXO)
00901-0009	JACK PIN JACK DPAM-9601E	1.0 /1	PCS	JP401
00901-0015	JACK DC POWER DDAE-9637	1.0 /1	PCS	JP402
00903-0015	PCMCIA DECK (52493-250CA)	1.0 /1	PCS	
00906-0021	CON WAFER 5267-10A	2.0 /1	PCS	JP13,15
00906-0035	CON WAFER 5267-14A	1.0 /1	PCS	JP3
00906-0042	PCMCIA WAFER 91931-31169	2.0 /1	PCS	JP5,6
00906-0043	CON WAFER 5267-12A	1.0 /1	PCS	JP12
00906-0047	CON WAFER 52045-3445	1.0 /1	PCS	JP10
00906-0048	CON WAFER 52368-0401	1.0 /1	PCS	JP9
00999-0018	CON SCART 2201-42RT DOUBLE	1.0 /1	PCS	U401
00999-0021	CON D-SUB 9PIN (5504F1-09P-02-02)	1.0 /1	PCS	JP403
01004-0089	PCB CPU B/D(SUPERSET) REV 1.5	1.0 /1	PCS	
01100-0002	INDUCTOR 1.2uH/3PI/AXIAL	3.0 /1	PCS	L10,22,409
01100-0009	INDUCTOR 270uH/5PI/RADIAL	2.0 /1	PCS	L2,6
01103-0004	CHIP BEAD-601 CIM21U601NE	30.0 /1	PCS	L3-5,11-21,24-30,32,33,57,403-407,R185
01103-0005	POWER BEAD CIB21P330NE	2.0 /1	PCS	L7,8
01200-0002	FILTER EMI NFM51R10P107	1.0 /1	PCS	F1
01405-0003	RF MODULATOR MDLP3E503A	1.0 /1	PCS	U402
1015201802	SCREW B/H NAT(M2*18)	4.0 /1	PCS	ASSY CPU B/D+PCMCIA DECK
10501-0590	LABEL BAR-CODE	1.0 /1	PCS	
010-0092	ASSY FEC B/D (SUPERSET:TDA 8044 적용 B/D)			
00009-0001	IC REGULATOR 7805/TO-220	1.0 /1	PCS	U601
00010-0029	IC QPSK DEMODULATOR TDA8044AH/C2/QFP100	1.0 /1	PCS	U603

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MODEL CODE 15-002 F1-VACI(SUPERSET)

CODE	NAME	Q'TY	UNIT	LOCATION
00106-0002	CAP MULTI CERAMIC-CHIP 0.1uF/104p/25V/X7R/2012	4.0 /1	PCS	C609,610,613,614
00106-0014	CAP MULTI CERAMIC-CHIP 27pF/270p/50V/C0G/2012	1.0 /1	PCS	C622
00106-0025	CAP MULTI CERAMIC-CHIP 0.1uF/104p/50V/Y5V/2012	2.0 /1	PCS	C604,615
00106-0042	CAP MULTI CERAMIC-CHIP 0.1uF/104p/25V/Y5V/1608	11.0 /1	PCS	C602,603,605,606,608,611,616,618,619,624,648
00106-0053	CAP MULTI CERAMIC-CHIP 0.01uF/103p/25V/X7R/1608	1.0 /1	PCS	C633
00106-0055	CAP MULTI CERAMIC-CHIP 0.0068uF/682p/25V/X7R/1608	11.0 /1	PCS	C617,625-632,635,638
00106-0090	CAP MULTI CERAMIC-CHIP 27pF/270p/25V/C0G/1608	1.0 /1	PCS	C621
00107-0061	CAP ELE 0.68uF/50V/SSL	1.0 /1	PCS	C601
00107-0067	CAP ELE 47uF/50V/SSL	1.0 /1	PCS	C612
00107-0083	CAP ELE 100uF/10V/SSL	5.0 /1	PCS	C607,623,634,636,637
00200-0087	RES CHIP 4.7K, 5%, 1608	4.0 /1	PCS	R607,609,612,615
00200-0088	RES CHIP 470, 5%, 1608	2.0 /1	PCS	R604,611
00200-0090	RES CHIP 0, 5%, 1608	1.0 /1	PCS	R637
00200-0091	RES CHIP 10, 5%, 1608	1.0 /1	PCS	R630
00200-0092	RES CHIP 1.2K, 5%, 1608	1.0 /1	PCS	R603
00200-0093	RES CHIP 22K, 5%, 1608	1.0 /1	PCS	R608
00200-0095	RES CHIP 1M, 5%, 1608	1.0 /1	PCS	R616
00200-0096	RES CHIP 10K, 5%, 1608	3.0 /1	PCS	R605,639,641
00200-0098	RES CHIP 47, 5%, 1608	11.0 /1	PCS	R618-628
00200-0121	RES CHIP 2.7K, 5%, 1608	1.0 /1	PCS	R610
00200-0142	RES CHIP 2.2K, 5%, 1608	2.0 /1	PCS	R606,614
00200-0182	RES CHIP 3.9, 5%, 3216	1.0 /1	PCS	R601
00209-0001	RES FIXED CEMENT 100, 5W, 5%/AXIAL(L-TYPE)	1.0 /1	PCS	R602
00301-0017	DIODE ZENER TZM5240B(10V)/SOD80	1.0 /1	PCS	D603
00304-0001	DIODE SWITCHING KDS193/SOT-23	1.0 /1	PCS	D601
00305-0001	TVS DIODE P6KE30	1.0 /1	PCS	D602
00400-0007	TR CHIP KST4401/NPN/SOT-23	3.0 /1	PCS	Q602-604
00401-0012	TR NOMAL KSC2331-Y/NPN/TO-92	1.0 /1	PCS	Q601
00500-0022	VIBRATOR CRYSTAL 3rD OVERTONE 4.0625MHz/30PPM	1.0 /1	PCS	Y601
00906-0047	CON WAFER 52045-3445	1.0 /1	PCS	JP600
01004-0062	PCB FEC B/D(SUPERSET) REV 1.2	1.0 /1	PCS	
01100-0009	INDUCTOR 270uH/5PI/RADIAL	1.0 /1	PCS	L601
01102-0000	FERRITE BEAD-AXIAL 8.1mm/AXIAL	1.0 /1	PCS	L602
01103-0004	CHIP BEAD-601 CIM21U601NE	3.0 /1	PCS	L603,605,606
01301-0064	HARNESS FPC ASSY#73(50mm, 34LINE)	1.0 /1	PCS	ASSY CPU B/D+ASSY FEC B/D
01404-0002	TUNER SD1228/LA-MK2	1.0 /1	PCS	TN601
09900-0029	RELAY SY-6-K	1.0 /1	PCS	K601
10081-07-001	SHEET GLUE (3M TAPE #9890,12X18)	1.0 /1	PCS	U603 ACCESSARY
10081-09-001	INSULATION PAD (#4941,15X21X1t)	1.0 /1	PCS	R602 ACCESSARY(DO NOT USE WHEN USE R602 RES CEMENT L-TYPE)
10191-0080	HEAT SINK SY200 HAR SERIES	1.0 /1	PCS	U601 ACCESSARY
10591-02-001	HEAT SINK F1-CI	1.0 /1	PCS	U603 ACCESSARY
1105300804	SCREW T/T 2S B/H BLK (03*8)	1.0 /1	PCS	U601 ACCESSARY

020-0088 ASSY FRONT F1-VACI

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MODEL CODE 15-002 F1-VACI(SUPERSET)

CODE	NAME	Q'TY	UNIT	LOCATION
010-0043	ASSY FRONT B/D F1-CI	1.0 /1	PCS	
020-0087	ASSY SUB FRONT F1-VACI	1.0 /1	PCS	
1105300802	SCREW T/T 2S B/H NAT (03*8)	5.0 /1	PCS	ASSY FRONT+ASSY FRONT B/D(5EA)
050-0071	**ASSY BOTTOM F1,F1-CI,F1-VA,F1-VACI(SUPERSET)**			
050-0067	ASSY LEG F1,F1-CI,F1-VA,F1-VACI	1.0 /1	PCS	
10031-06-008	CASE BOTTOM (SUPERSET-SMPS TYPE)	1.0 /1	PCS	
060-0004	**ASS'Y POWER S/W(WITH HARNESS #82)**			
00800-0001	POWER SW (JRA1102K)	1.0 /1	PCS	
010-0043	**ASSY FRONT B/D F1-CI**			
00107-0068	CAP ELE 47uF/16V/SSE/BULK	2.0 /1	PCS	C3,4
00107-0077	CAP ELE 100uF/6.3V/SSE/BULK	1.0 /1	PCS	C2
00203-0000	RES CARBON 10,1/4W,5%	1.0 /1	PCS	R10
00203-0003	RES CARBON 10K,1/4W,5%	1.0 /1	PCS	R1(DO NOT USE WHEN REMOCON SENSOR IS LITEON (LTM-97AT-38W))
00203-0017	RES CARBON 22,1/4W,5%	8.0 /1	PCS	R2,3,4,5,6,7,8,9
00203-0024	RES CARBON 330,1/4W,5%	1.0 /1	PCS	R11(DO NOT USE WHEN REMOCON SENSOR IS LITEON (LTM-97AT-38W))
00203-0061	RES CARBON 47, 1/4W, 5%	1.0 /1	PCS	R11(DO NOT USE WHEN REMOCON SENSOR IS TEMIC 5380)
00401-0010	TR NOMAL 2SC1741S/NPN/SPT	8.0 /1	PCS	Q1,6,7,8,9,10,11,12
00401-0011	TR NOMAL 2SA854S/PNP/SPT	4.0 /1	PCS	Q2,3,4,5
00603-0001	7-SEGMENT LED DISPLAY LTC-5623G-12(높이4mm)	1.0 /1	PCS	U2
00802-0000	S/W TACT KPT-1105A/4pin/6*6(BULK)	3.0 /1	PCS	S1,2,3
01004-0026	PCB FRONT F1-CI REV 1.1	1.0 /1	PCS	
01301-0051	HARNESS ASSY#60 2GH060	1.0 /1	PCS	JP1
01301-0052	HARNESS ASSY#61 2GH061	1.0 /1	PCS	JP2
09900-0001	JUMPER JUMPER 0	4.0 /1	PCS	J1,2,3,4
09900-0042	REMOCON SENSOR LTM-97AT-38W	1.0 /1	PCS	U1
10111-04-001	SUPPORT CUSHION F1,F1-CI (10*10*5.3T)	1.0 /1	PCS	(DO NOT USE WHEN REMOCON SENSOR IS LITEON (LTM-97AT-38W))
020-0087	**ASSY SUB FRONT F1-VACI**			
10001-05-003	PANEL FRONT F1-VACI	1.0 /1	PCS	
10051-08-001	KNOB POWER F1-CI	1.0 /1	PCS	
10051-09-001	KNOB DIRECTION F1-CI	1.0 /1	PCS	
10061-02-004	DOOR F1-VACI	1.0 /1	PCS	
10071-05-001	WINDOW F1-CI	1.0 /1	PCS	
10171-01-002	BADGE HUMAX (7X28.5)	1.0 /1	PCS	
050-0067	**ASSY LEG F1,F1-CI,F1-VA,F1-VACI**			
10161-04-001	LEG FOOT (LOCKING TYPE)	2.0 /1	PCS	